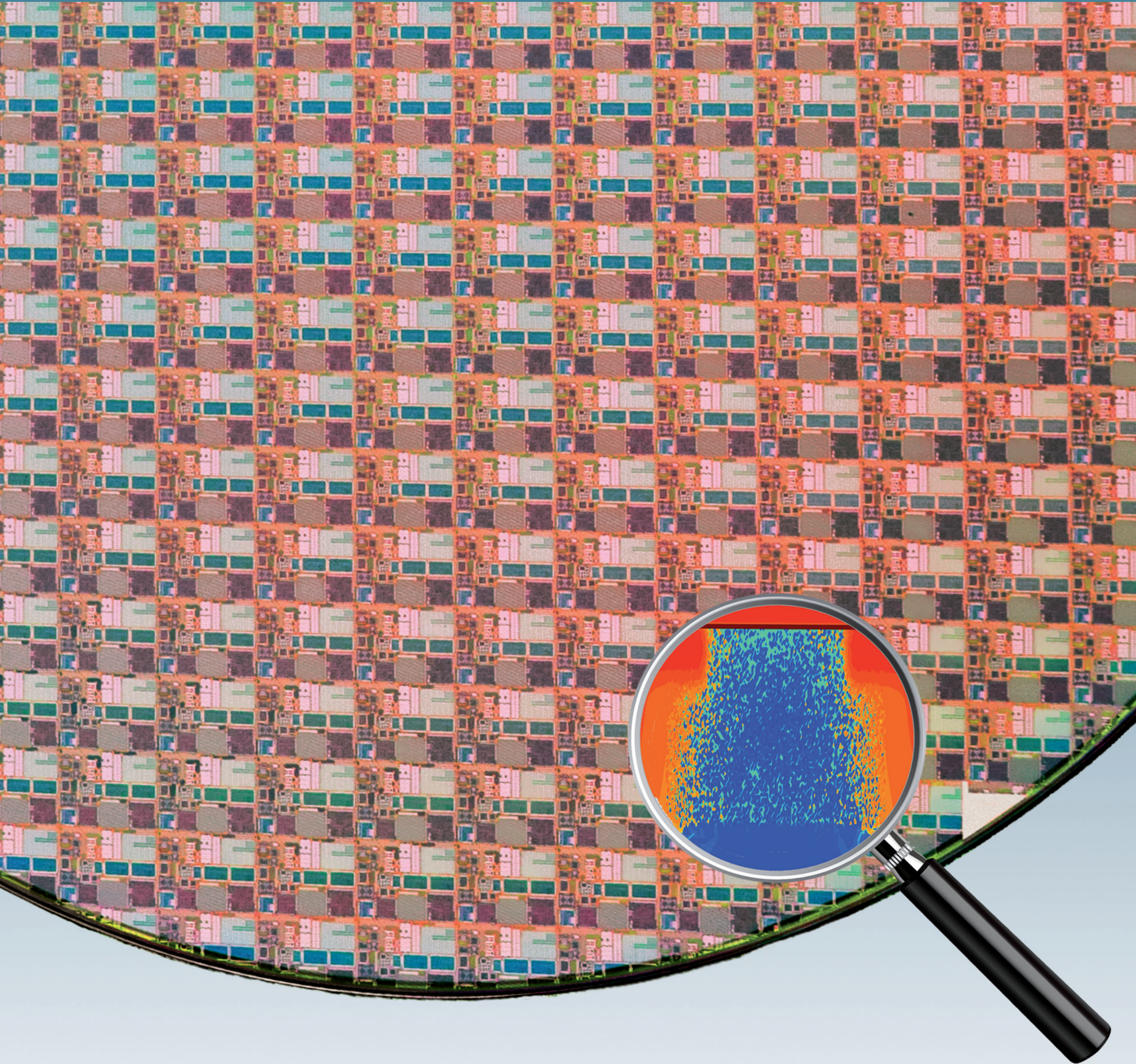
Interpretation of MOS transistor mismatch signature through statistical device simulations



Pietro Andricciola

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DISSERTATION

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There's no sense in being precise when you don't even know what you're talking about.

John von Neumann

To my families

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Chapter 1

Introduction

Semiconductor manufacturers daily fabricate millions of nominally identical integrated circuits made of supposedly identical components. However controlled the fabrication process can be, two components will always be slightly different when thoroughly compared. The comparison between two components is usually done using a certain parameter as estimator of the integrated circuit (IC) or transistor performance, e.g. a frequency of an oscillator or a current delivered by a transistor. What happens in reality is, for instance, that the frequencies of the identical oscillators fabricated, with the same process but in different foundries, or in different moments in the same foundry, will be different. Actually, even chips fabricated on the same wafer will not be exactly the same, as some fundamental characteristics of the fabrication process vary across the wafer. These sorts of variability are often deterministic. This means that a clear pattern appears after a significant number of observations.

Let us consider the following example where the resistance value of a resistor varies wafer after wafer. The median value of this resistance for wafer 1 is 51 Ω while for wafer 2 is 52 Ω and so on, with the resistance that slightly increases wafer after wafer. This could be an indication of a change (gas flow, temperature, pressure) that is happening in one of the machines used to fabricate these resistors. With a proper monitoring and feedback this trend can be compensated.

The same applies to parametric gradients across a wafer. If the differences among the values of the resistor are consistent with the position on the wafer it means that some process parameters are position dependent inside the machine and the technologist can tune the machine to reduce the variation to the

minimum. The process will be released for designing electronic circuit with a nominal value per parameter and a certain window around it. The circuit and layout implementation final design must assure that the chip will work for any value of that parameter, given that it is within the process window provided.

Last but not least, there is the variability on the smallest length scale that includes the differences between supposedly identical components within the same chip. This is typically indicated with the term **mismatch** or **matching**. Differently from the other types of variability mentioned above, mismatch is usually random; it can therefore not be adjusted and compensated during the fabrication. Random mismatch is generally attributed to microscopic device architecture fluctuations, e.g. the fluctuation of the position and the number of dopants in a transistor (controlled by stochastic processes) [1]. A key element of the discussions about matching, or variability associated with microscopic stochastic fluctuations, is that the equality between supposedly identical components becomes better when the devices are made larger (the fluctuations average out) [2].

Although the mismatch represents only a part of the total variability that can be measured on multiple wafers, it is, in many cases, a performance limiter. For a correct functionality of an integrated circuit (IC), identically designed components fabricated on the same circuit need to have the same performance. As a matter of fact, complex circuits base their functionality on simpler, but fundamental, circuit blocks. Many of such blocks, e.g., bandgap references, current mirrors, differential amplifiers etc., rely on the availability of multiple **identical** active and passive components. But as already argued, two allegedly identical components will never be exactly the same.

The following example of a current mirror demonstrates how mismatch affects the function of a simple block. In figure 1.1 a schematic representation of such circuit is drawn. The purpose of this circuit is to replicate the reference current (I_{ref}) in order to supply it to other parts of the IC. The reference current is usually obtained through a complicate circuitry that stabilizes the current making it robust against supply voltage and temperature variations. The n devices represented in figure 1.1, M1, M2 and so on to Mn, have the gate and source terminals connected together. This means that if M2 (or Mn) and M1 are nominally identical, the current that will flow in M2 (Mn), I_{out}, should be an exact replica as the current that is forced into M1, I_{ref}. In reality I_{out} and I_{ref} will always be different, as M2 (Mn) and M1 will always be microscopically different.

Using a simple three-stage circuit for signal processing, it has been shown that the mismatch is the limiting factor for the overall performance of the whole circuit [3]. The performance of such a circuit is judged by looking at its ac-

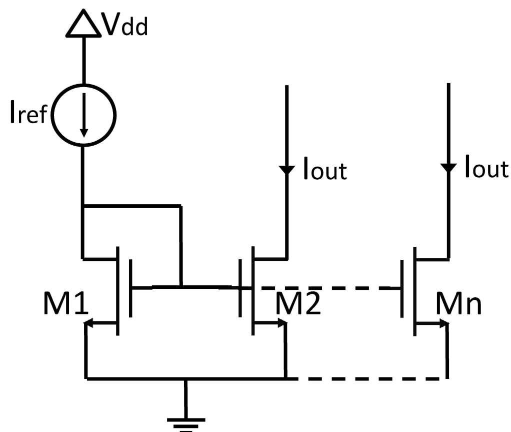


Figure 1.1: Schematic representation of a current mirror. This fundamental block is needed to replicate a reference current and bring it to other parts of the chip.

curacy, speed and power consumption. The accuracy is strongly dependent on the mismatch and improves with larger transistors. Apart from the additional cost that larger transistors would bring along, also the other two performance indicators will suffer from the choice of big transistors. In case of CMOS, a wider transistor results in higher current, thus increasing the speed but also power consumption, while a longer transistor reduces the current, thus the power, but increases its capacitance slowing down the chip. The design choice will be a trade-off between these performance indicators and it is limited by the matching properties of the technology [3].

In the past, when electronic system design was dominated by vacuum tubes and discrete components, the realization of a circuit was done by handpicking transistors and passive elements and connecting them together. It was therefore possible to choose (‘match’), from the same kind of components, the one that had the closest performance to the design specifications and be sure that the final result had a perfect matching. Of course, this cannot be done for an IC with the current process technology.

From the variability point of view, a working IC is a challenge that spans across at least three different levels. One is the process technology: the fabrication process should be such that its variability remains below manageable levels. Another one is the characterization and modeling of the mismatch properties, because only with good models and reliable estimators is possible

to make accurate predictions. Finally, the third area is the circuit design; the circuits need to be robust against the variations foreseen by the models. Without a combined effort in all these three fields, the fabrication of contemporary working IC would not be successful.

This thesis contributes predominantly to the second task: it aims at expanding the understanding and the characterization of mismatch of modern Metal Oxide Semiconductor (MOS) transistors. The investigation is done with device simulations and high-precision measurements. In the following sections the simulations, the characterization and the modeling of the MOS transistor mismatch are briefly summarized.

1.1 TCAD and mismatch

In the past decades, computer aided device and process simulations, generally called TCAD, have become very important tools of the semiconductor industry. The improvements in the accuracy of the device-physics description, the development of efficient multidimensional equation solvers and the increasing availability of 'low-cost' computational power transformed the use of TCAD simulations from mere support to an indispensable R&D tool, especially in early stage of technology development [4, 5]. TCAD is also used by modeling experts and device physicists to obtain better understanding of the physical behavior of the device and to investigate unforeseen behavior encountered in actual device measurements. TCAD simulations have been also used to confirm mismatch relations and investigate the impact of sources of fluctuations, especially Random Dopant Fluctuations (RDF). A clear example of how to use device simulations to confirm analytical model is given by the study of the impact of RDF on threshold voltage mismatch in MOS transistors carried out by Stolk *et al.* [6]. With a 2-D drift diffusion simulation they validated their model of the threshold voltage fluctuation in a uniformly doped transistor. Taking into account the fluctuations of the surface potential and the electric field they confirmed and refined the work of Pelgrom *et al.* [2]: the standard deviation of the threshold voltage fluctuation is inversely proportional to the square root of the active area and proportional to the fourth root of the doping concentration (see equation 4.1 in chapter 4 for the complete formulation).

Furthermore, in the last decades, device simulation has been extensively developed and improved to enable analysis of the random variability of device performance [7, 8, 9, 10, 11]. In that respect, many efforts, such as from the group of Device Modeling at Glasgow University, went into adding sources of variability to Drift-Diffusion (DD) as well as Monte Carlo (MC) based simula-

tors [12, 13].

DD simulations play the role of the work-horse in semiconductor R&D because of the very good trade-off between speed and accuracy. It proved possible to study the effect of RDF, Line Edge Roughness (LER), Poly-Grain Boundaries (PGB) and several other factors, in contemporary and future technology nodes [12, 14, 15]. For example, the contribution of RDF and LER was investigated in transistors of less than 20 nm of channel length, showing that both contributors would have a dramatic effect on the functionality of the device and the resulting circuits built with them. This represents a proof of the need for a different architecture of the transistor (a drive for 3-D transistor structure), alternative gate composition, and/or a more advanced lithography tool (a drive for Extreme Ultra Violet source).

In this thesis the approach is different. This research was carried out in the process technology laboratory of NXP Semiconductors [16]. During the years of this study, NXP did not focus its strategy on the development of future CMOS nodes and therefore on the analysis of the variability associated with those, but reinforced strong interests in high-performance mixed-signal circuits [17] largely based on NXP's Philips heritage in analog and mixed-signal product lines. This research led to a better understanding of the mismatch causes and dynamics in existing, production ready, technologies (somewhat larger devices). For this task, it proved crucial to have a tool that allows studying the impact of different sources of mismatch on transistor behavior and compare those with measurements and models. Developed in a collaboration between Uppsala University and Philips Research [18], the `Simulated Statistical Parameter Extraction Tool (SiSPET)` is the tool that has been used (and expanded) throughout this thesis to investigate MOS transistor mismatch. It consists of a 2-D DD device simulator, a randomizer used to insert sources of variability in the nominal virtual device and various scripts and several routines for data analysis and parameter extraction.

A tool like SiSPET is aimed at two main results. In the first place, shortcomings in existing mismatch models can be identified, understood and perhaps overcome. This, in turn, will raise the confidence in models circuit designers can use for cutting edge solutions and will reduce both the number of necessary design spins for a fully-functional circuit, as well as the silicon area needed to fulfill the mismatch requirements. Second, a tool capable to deal with device variability represents a first-line help in cases of yield issues or unexpected behavior. If a circuit malfunction is attributable to random variations, a tool like SiSPET can confirm or reject the hypothesis in relatively short time without expensive silicon experiments. The merits and limitations of this tool are discussed in this thesis.

1.2 Mismatch model

Although mismatch becomes worse when device dimensions reduce, which means it is becoming every day more important, one of the first investigations of the impact of threshold voltage fluctuations on MOSFET technology was published already roughly 40 years ago, in 1972, by Hoeneisen and Mead [19].

The golden age of the literature about mismatch is probably the 80's. In fact, in 1984 the first model for MOS transistors that included a dimensional dependency was proposed by Shyu *et al.* [20]. That work was experimentally confirmed and expanded by Lakshmikumar *et al.* [21] in 1986. Three years after that, Pelgrom *et al.* [2] derived a general model, independent from the causes of mismatch, that mathematically describes the dimensional dependence of MOS transistor random mismatch (and it was found to hold also for all components that fall under their assumptions). This work resulted in the so-called "Pelgrom law" and it can be summarized as follows.

The differences between two electronic components are estimated through the measurement (or extracted via a model) of an electrical parameter P, e.g., resistance, current, voltage etc. If the dimensions of the underlying physical causes of these parametric changes are small with respect to the device dimensions, and mutually independent, the mismatch fluctuation standard deviation $\sigma_{\Delta P}$ (or $\sigma_{\Delta P/P}$ if the parameter variations should be considered in relative values) of an electrical parameter P scales with the inverse of the square root of the device area, in symbols:

$$\sigma_{\Delta P} = A_{\Delta P}/\sqrt{W \times L} \tag{1.1}$$

or

$$\sigma_{\Delta P/P} = A_{\Delta P/P}/\sqrt{W \times L} \tag{1.2}$$

where W and L are the effective dimensions of the active region of the device. The A-factor $A_{\Delta P}$ (or $A_{\Delta P/P}$), often referred to as Pelgrom-factor or area factor, is characteristic of a technology and in first approximation describes the mismatch properties of a parameter for a particular technology. One of the most remarkable observations about these microscopic parametric mismatch fluctuations is that, under the assumptions introduced by Pelgrom *et al.*, the behavior described by the equation 1.1 is encountered for all integrated circuit device types and for most of their observables or parameters. This relatively simple equation can give an idea of what is the order of magnitude of contemporary mismatch. Let us assume that a technology has an area factor for

the threshold voltage mismatch of 3 mVμm and the transistor dimensions are $L = 0.04\ \mu$m and $W = 0.2\ \mu$m. The resulting standard deviation of the relative drain current mismatch is $\sigma_{\Delta V_{\mathrm{T}}} \approx 33$ mV. In large ICs, with millions of components, the calculation of the possible variation of the drain current for this technology needs to be done on four or five sigmas. In this case, the design should be robust against variations that can reach $\pm$ 150 mV, that is a substantial part of the supply voltage. This example explains why the scientific community, as well as the design and manufacturing communities, are dedicating much attention to the problem of mismatch.

Despite the usability of the model proposed by Pelgrom (which is limited by its fundamental assumptions), many other models have been published over the years. For example, Croon [22] and Drennan *et al.* [23], in different studies, focused their modeling efforts on drain current mismatch on the full bias range. Croon provided a physically-based drain current model that correctly described drain current mismatch by separating the contribution of the threshold voltage mismatch and the current factor mismatch. A broader approach was followed by Drennan which, with a technique called Back Propagation of Variance (BPV), linked the drain current mismatch to numerous independent process parameter variations. By doing so, he obtained a matrix of sensitivities of the drain current with respect to each of the process parameters of a particular technology node.

In recent years, the group of Takeuchi proposed a new geometry scaling model, different from Pelgrom's by adding some extra technology-related parameters which trends give an idea of the effect of different sources of mismatch among different technology nodes [24, 25].

1.3 Characterization and experiments

As it is in any science, actual experiments, measurements and analysis method need to be produced to prove theory and quantify effects. Mizuno *et al.* were one of the first to publish an experimental study on the threshold voltage fluctuation due to random dopant fluctuations based on large population of devices [26]. Several experiments have been performed over the years on the impact of certain process conditions on the mismatch. A good example of these experiments is the study of the impact of metal coverage, and gate depletion with boron penetration on MOS transistor mismatch, both published by Tuinhout *et al.* [27, 28]. Many other contributions about test structures and analysis methods appear regularly at the International Conference on Microelectronics Test Structure (ICMTS) [29]. Other examples of the kind of

contributions that help device scientist to better deal with the characterization of subtle mismatch effects are the comparison of five different methods of threshold voltage extraction (among which one was proven to be the best one, yet with many shortcomings) [30] and the analysis of an abnormally high electrical fluctuations in heavily pocket[1] implanted transistors [31].

Beside good test structure and well designed experiments, a good mismatch analysis needs to be free from misconceptions that can lead to wrong conclusions. An example of such misconceptions is the use of relative threshold mismatch, $\Delta V_\mathrm{T}/V_\mathrm{T}$, when comparing mismatch properties of populations with different nominal threshold voltages. For instance, the variation of the relative threshold voltage has been used for mismatch analysis in cases of threshold voltage change due to different temperatures or different body biases [32, 33]. This is incorrect for the following reasons. First, if the threshold voltage goes to zero, the relative quantity, $\Delta V_\mathrm{T}/V_\mathrm{T}$, yields an infinite mismatch, so this definition is not applicable to "normally on" and so-called native devices. Second, the approach with relative threshold voltage mismatch is misleading. As a matter of fact, an increase in the relative threshold voltage mismatch results in a reduction of the drain current mismatch. For example, for $V_\mathrm{ds} \gg (V_\mathrm{gs} - V_\mathrm{T})$, the drain current (in saturation) can be expressed in its simplest form by:

$$I_\mathrm{d} = \frac{\beta}{2}(V_\mathrm{gs} - V_\mathrm{T})^2 \tag{1.3}$$

where β is the current factor. This leads to an expression of the variance of the relative drain current mismatch that reads:

$$(\sigma_{\Delta I_\mathrm{d}/I_\mathrm{d}})^2 = \frac{4(\sigma_{\Delta V_\mathrm{T}})^2}{(V_\mathrm{gs} - V_\mathrm{T})^2} + (\sigma_{\Delta\beta/\beta})^2 \tag{1.4}$$

with obvious meaning of all the symbols. The first term of the right-hand side of equation (1.4) is proportional to the variance of absolute threshold voltage mismatch and inversely proportional to the square of the gate overdrive $V_\mathrm{gs} - V_\mathrm{T}$. Thus, for the same gate bias and same absolute threshold voltage mismatch, when the threshold voltage reduces the overdrive increases, consequently diminishing the contribution of the threshold voltage mismatch to the overall drain current mismatch. The use of relative threshold voltage mismatch would give the exact opposite result: to a larger relative V_T mismatch will correspond a smaller relative drain current mismatch. This is rather counterintuitive.

Given these considerations, the threshold voltage mismatch should be always reported and analyzed in its absolute-value form. This example does

[1]The pockets are doping implants with a high angle of implantation used to overcome short channel effects in contemporary CMOS devices.

demonstrate how even with a very advanced simulation or a fully thought through experiment wrong results can easily be obtained if no proper analysis methods are used.

1.4 About this thesis

This thesis is the result of a Twente University PhD project carried out in the Device Modeling and Characterization group of NXP Semiconductors in Eindhoven. This project has been sponsored by the European Community through the Marie Curie Action MOICCO. The fact that the project was positioned between industry and university (as PhD program) led to a good balance between simulations and characterization work with an eye always directed to modeling and possible applications.

The study of internal and external factors influencing MOS transistor mismatch was born following the necessity of contributing something new to this field and of helping, at the same time, NXP designers with concrete feedback on how to obtain better products. It was therefore decided to focus on existing technology nodes already available in production, e.g., 65 nm minimum gate length, and on developing a software suite and a simple analysis methodology that would help in identifying possible mismatch problems and in distinguishing the different causes of mismatch.

These general directions converged into the study of:

- the impact of random dopant fluctuations and interface state fluctuations on MOS transistor mismatch, with the help of our simulation tool and an advanced measurement equipment;
- the impact of channel doping non-uniformity, interface state fluctuations and **series resistance fluctuations** on LDMOS transistor mismatch with our simulation tool trying to reproduce measurement results;
- the impact of temperature on MOS transistor mismatch across four technology nodes mainly with measurements and confirmed a theoretical explanation with simulations.

This thesis is thus structured as follows: first the simulation approach and the analysis methodology are explained in chapter 2.

The impact of interface state fluctuations on MOS transistor mismatch is investigated in the subsequent chapter. In that chapter the simulator is used to prove a measured device behavior believed to be caused by interface state fluctuations. Some elementary modeling work and very fast I-V pulsed

measurement have been performed and their results are discussed in the same chapter.

An application of our methodology to study LDMOS mismatch properties is discussed in chapter 4.

The temperature effect on MOS transistor mismatch across four different technology nodes is presented in chapter 5.

Finally, in chapter 6 the main conclusions are summarized.

Chapter 2

SiSPET and analysis methodology

This chapter is about the software and tools used during this research activity. It starts by outlining the essential characteristics of our main tool: `SiSPET (Simulated Statistical Parameter Extraction Tool)`. Then, the implementation of the different sources of fluctuation that are built into the tool is explained. In the next section "TCAD calibration", the procedure to obtain a good simulated replica of an actual transistor is discussed. Finally, the data analysis methodology used throughout this thesis is described.

2.1 TCAD and SiSPET

SiSPET is a tool for the evaluation of the influence of mismatch sources on the device behavior and also on compact models. It was developed in a collaboration between Uppsala University and Philips Research [18]. SiSPET consists of a suite of commercially available programs for device simulation (Synopsys) and data analysis (mostly Matlab [34]), a model parameter extraction tool (implemented through ICCAP [35]) and a microscopic device architecture randomizer (`dr`). Although some solutions to introduce sources of fluctuation, usually RDF, are already implemented at a higher level as noise disturbances in some simulators, e.g. Sentaurus Device (SD) [36], a true device randomizer was developed in-house and used for the study. This provides a higher flexibility and better control, and the possibility to trace back and exactly reproduce any

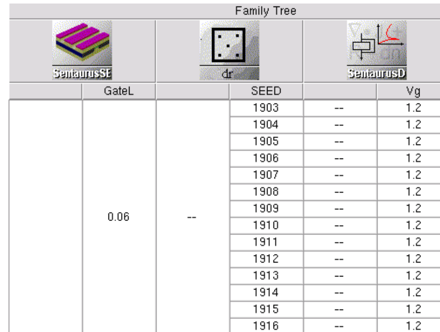
randomized device. The simulation framework of SiSPET is described here, leaving the analysis methodology for the end of this chapter while the model parameter extraction is discussed in detail in chapter 3.

The analyzed devices were not generated through process simulations, but were created using the `Sentaurus Structure Editor` (SSE) [37]: it allows the creation of any structure with different kinds of material and doping concentration. SSE is preferred over a process simulator because it is much faster and it provides a better controllability of the actual device construction (down to a single grid point). In any case, this study was not meant to investigate the influence of process steps on mismatch but to analyze device architecture and resulting fluctuations of electrical device properties.

For extensive statistical device simulation, the main characteristics that the simulator needs to have are speed, accuracy and availability of standard models. Although it is widely published that a Monte Carlo simulation approach yields the best accuracy, especially for very short transistors, the time needed to complete a simulation can be very long. Several attempts of using MC simulations for statistical variability have been reported [13], but those studies all analyze extremely small transistors. In this study, several, relatively large device sizes of a technology have been simulated. This was largely the results of the strategy of NXP, which mainly focused its product portfolio towards high-performance mixed-signal circuits. Since statistical simulations are needed, i.e., many simulation instances, a faster but "accurate enough" approach is preferable. Given these requirements, the devices (before and after randomization) were simulated with `Sentaurus Device` a commercial drift-diffusion device simulator from Synopsys [36] in its two-dimensional (2-D) version.

The device randomizer, basically the heart of SiSPET, is based on a series of scripts and programs written in **Ruby** [38], an open-source programming language. Although during the course of the research several modifications were made to the programs, especially to add new sources of variation initially not implemented, the basic structure remains the same as originally built [18]. The basic idea is that the randomizer manipulates the input files of the device simulator. One can therefore modify in a controlled manner any device characteristic, e.g. a doping concentration associated with a grid point or a resistance value in the electrode definition.

The procedure is basically as follows: first the unperturbed device is created and calibrated to assure realistic I-V curves, then the resulting data file, describing the device, is used as input to the randomizer after which multiple microscopically different devices are created and subsequently simulated. The user interface of the randomizer is inserted into the `Sentaurus WorkBench` (SWB) [39] that allows the feeding of variables and parameters to the various



Family Tree

SentaurusSE		dr		SentaurusD	
	GateL		SEED		Vg
	0.06	--	1903	--	1.2
			1904	--	1.2
			1905	--	1.2
			1906	--	1.2
			1907	--	1.2
			1908	--	1.2
			1909	--	1.2
			1910	--	1.2
			1911	--	1.2
			1912	--	1.2
			1913	--	1.2
			1914	--	1.2
			1915	--	1.2
			1916	--	1.2

Figure 2.1: Screen shot of a part of a WorkBench project including the randomizer `dr`.

programs through the user interface and a smooth interaction of user-defined programs and Synopsys elements. In figure 2.1 a screen shot of the WorkBench with a typical SiSPET project is shown. The gate length of the device (GateL variable in the SSE part on the left), the randomizer seed number (SEED in the `dr` section in the middle) and the maximum gate voltage (V_{g} for SD on the right) are the modifiable variables in this example.
The randomizer used in this tool is based upon a pseudo-random number generator [40] and the seed represents a key to generate a unique and repeatable sequence of pseudo-random numbers. Using the same seed, one can recreate the exact same sequence of random numbers as created the first time. This is an important feature to be able to trace back each perturbed device in relation to the created device architecture change. The sequence of pseudo-random numbers are used to add stochastic variations (dopant number, oxide traps etc.) to the 'nominal' device. The implementation of the specific sources of fluctuations investigated within this research project is described in the next section.

2.2 Sources of mismatch

Parametric mismatch fluctuations measured on dedicated test structures are generally the final result of a combination of multiple sources of fluctuation. In order to obtain a better understanding of the mismatch behavior of the device it is of fundamental importance to analyze the individual causes in detail. Statistical simulations represent an easy and fast way (in fact probably the only viable way) to study the effect of **controlled** mismatch causes in modern MOS

device architectures.
There are examples of very well controlled experiments (see [28] for an experiment of the impact of boron penetration on mismatch) but they are certainly very expensive and are not always successful. One may argue that the use of a compact model is a very fast and inexpensive way to see the effect of individual sources of mismatch as well. A compact model is an analytical model that, based on the physics of the device through compact equations, describes quite accurately the behavior of the device. The shortcoming of compact models, however, comes with the fact that often not all the quantities in the equations are linked to each other through actual physical relations. Also the approximations made to make the model "compact" might be such that subtle mismatch signatures will not be captured.
In particular, the main goal of research activities in this field should be aimed at identifying the most important sources of mismatch and verifying how these affect the device variability and interact with each other. The main cause of mismatch in MOS technologies is believed to be the random dopant fluctuations. For instance, it has been shown that RDF explain roughly 60 % of the total mismatch in a 65-nm technology node [41]. However, in order to create a complete description of the device behavior, other sources of mismatch are essential. As mentioned in chapter 1, LER and PGB are those that attracted the most attention [14, 15, 42]. For their importance in the weak inversion operation region of the device, Random Interface state Fluctuations (RIF) are proposed here in this thesis as one of the most important source of variability in MOSFET mismatch after RDF [43]. Furthermore, a third source, especially important when the device operates with elevated currents is discussed in this thesis: the Random Series Resistance fluctuations (RSR). In fact, it can mimic either an incidental metalization asymmetry or a fluctuating probe-to-pad contact resistance [44].

2.2.1 Random Dopant Fluctuations

The implementation of RDF in a drift-diffusion simulator presents a series of challenges and compromises, very well described (and mostly solved) by G. Roy in [45]. For this particular implementation some of those challenges had to be faced again to assess the capabilities and limitations of our own tool.

One basic assumption of the implementation of the doping randomization is that the positions of impurities on an atomic scale are not correlated, therefore the number of dopants in a given volume follows a stochastic Poisson distribution [1]. For simplicity, the volume and thus the assignment of the random dopants is strictly linked to the grid (mesh) generated by the Synopsys tool.

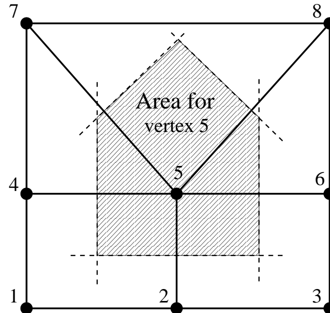


Figure 2.2: Illustration of the area calculation for a generic vertex. The numbers represent the labeling of the vertexes as done by Sentaurus. This area will be multiplied by a virtual width obtaining the volume associated with the grid point number 5.

The volume is calculated by multiplying the area that surrounds the grid point with a virtual width (depth), typically 1 μm. The area is calculated applying the shoelace algorithm [46] to a polygon obtained with the interception of the mid-point perpendiculars of the edges which connect the grid point to the adjacent ones (see figure 2.2). The number of dopants in a volume is:

$$n \;=\; N \cdot Area \cdot z \tag{2.1}$$

where N is the concentration of impurity atoms, $Area$ is the area associated to the grid point and z is the virtual depth of the device. The number n, thus obtained, is the nominal number that will be randomized following a Poisson distribution, yielding $\tilde{n}$ and then reconverted in impurity concentration, $\tilde{N}$. This concentration is then reassigned to the original grid point. This results in an adapted version of the Nearest Grid Point method [47]. When the grid is very dense, especially close to the oxide interface, where a very fine mesh is required for a proper device simulation, it can happen that the nominal number of dopants in a given volume is less than one. In that case the Poisson random number generator will often return a zero as result. This is a situation that must be avoided. Drift-diffusion simulators, in particular their mobility models, rely on the fact that the doping does have realistic values, typically between $1 \cdot 10^{14}$ cm^{-3} and $1 \cdot 10^{20}$ cm^{-3}. Outside of this range the simulator might give unrealistic results.

An example of a cross-section of a MOSFET after randomization using $z = 1$ μm is represented in figure 2.3. Many areas are visible with very low

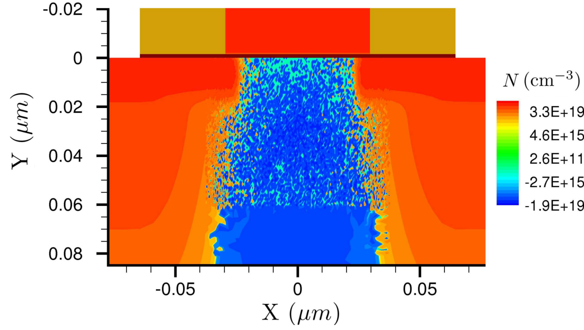


Figure 2.3: Cross-section of a MOSFET after applying the randomization using 1 μm as virtual depth. The upper part of the channel of the randomized device presents many 'zero' (green) areas.

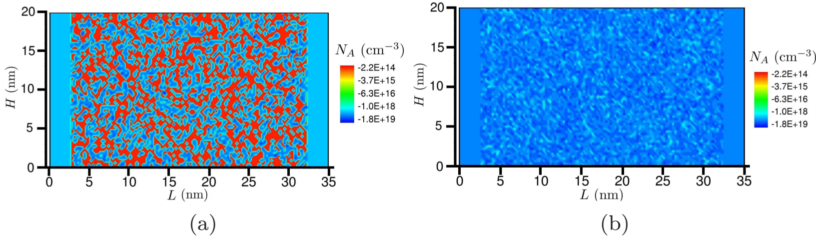


Figure 2.4: Doping concentration for two randomized resistors with two different widths 1 μm (a) and 10 μm (b). Red areas in (a) correspond to zero doping.

doping corresponding to grid points that correspond to zero dopant after randomization (green regions).

An example: a resistor

A simulation example of a simple resistor demonstrates quite well what happens in this unfavorable situation. Consider a piece of silicon of 20 nm×35 nm×1 μm (H×L×W) p-type doped with boron at a concentration of $5{\cdot}10^{18}\text{cm}^{-3}$. The dopant randomization is applied to it using three virtual widths, namely 1, 10 and 50 μm, generating populations of 51 samples for each width (W is perpendicular to the figure). A region of 5 nm either end was left unperturbed to ensure good contact with the electrodes. In figure 2.4 examples of resulting

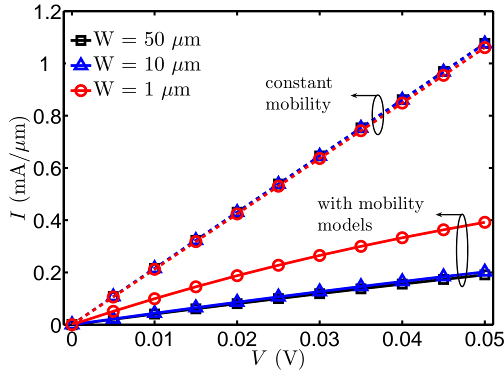


Figure 2.5: Median currents resulting from a simulation of 51 randomized resistors applying different virtual width (W). Mobility models are very sensitive to large doping concentration variations. W = 10 μm represents a good choice for this doping level.

resistors are shown for W = 1 μm and 10 μm. As expected, the resistor with W = 1 μm shows many 'zeros', red regions, while the resistor with 10-μm width appears quite smooth (a very similar picture is obtained using 50-μm width). Two sets of standard I-V simulations are performed: one was done applying a constant mobility and one using a doping dependent mobility model. The mobility model used in this experiment is the Philips Unified Mobility [48] model for the doping dependency (`PhuMob` in SD). The medians of the simulated I-V curves, scaled with W for quantitative comparison, are plotted in figure 2.5. In the case of constant mobility the value of the resistance changes only slightly from the obtained value for W = 1 μm. The value used for the constant mobility of the holes is $\mu = 470.5$ cm^2/Vs which results in a resistance value for this piece of silicon of about 45 Ω. On the other hand, when the doping dependency mobility model is used the results are quite different. The effective resistance increases substaintially, whereas the resistor with W = 1 μm shows a much lower resistance (basically half) compared to the other widths. In fact, a resistivity value for this doping of 0.0145 Ω·cm as calculated with this online tool [49] yields a resistance of about 250 Ω, very close to the value obtained with the resistor with larger width. The areas with low doping will create paths with "faster" holes that grossly affect the overall current.

In conclusion, if one wants to use a drift-diffusion simulator and obtain reliable results across the full bias range employing its mobility models, abrupt variations (exaggerated values) of doping concentration should be avoided.

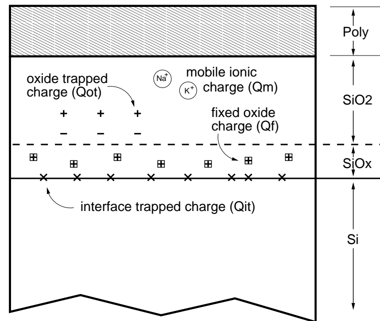


Figure 2.6: Terminology for charges associated with thermally oxidized silicon. After Deal [50].

Therefore, it was decided to always use a virtual width of at least 10 μm in our simulations to assure a reasonable number of dopants at each grid point. This limits the approach discussed in this thesis in using a fixed width. This implies however, that when comparing simulations and measurements, the simulation results are scaled with $\sqrt{\mathrm{W}}$. The drawback of this approach, also inherent to the use of a 2-D simulator, is the fact that it will not be able to capture narrow width effects and it will only be suitable for bulk MOSFET type of device architectures. As indicated in the introduction, this approach is in line with the more analogue and mixed-signal product strategy of NXP. In the following chapters, through the actual results, limitations of this approach will be investigated in more detail.

2.2.2 Random Interface state Fluctuation

A possible source of mismatch that can heavily affect the transistor behavior is the fluctuation of interface states. This was already introduced by Brews in 1972 [51]. The term interface-states is here used to indicate all the charges trapped at the interface between silicon and gate oxide (Q_{it} in figure 2.6). Fixed oxide charges, positioned in the bulk of the oxide, have not been considered in the simulations because, as shown by Putra *et al.* [52], they will not contribute significantly to mismatch. The main difference between fixed oxide traps and interface states is that the interface states, in the energy domain, occupy different levels in the band-gap: their charging state is thus dependent on the gate bias. Also, when the traps added to the device in the simulator are all with the same energy they will be filled (or emptied) all at the same gate

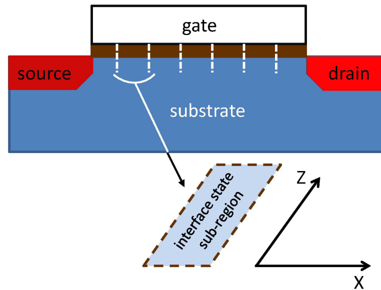


Figure 2.7: Schematic representation of a cross-section of a MOSFET and the implementation of interface states in it. The interface states are added to sub-regions in the oxide-silicon interface.

bias, dramatically reducing their impact on the variability. For a correct representation of this physical phenomenon, traps must be randomized in terms of concentration, energy and position along the interface [43]. The results of the investigation of the impact of interface state fluctuations will be discussed in depth in chapter 3.

The general approach for the implementation of interface state fluctuation in SiSPET can be described as follows. The interface between silicon and gate oxide is divided into sub-regions each 2-nm long covering the entire gate length (see figure 2.7). An energy value (E) is selected from the band-gap using a uniform probability density function. The nominal concentration (and therefore the number N obtained multiplying the concentration with the virtual width) is calculated from an empirical equation that mimics a realistic parabolic shape, e.g., $N = 60 \cdot E^2 + 40$ corresponding to a $2{\cdot}10^{-11}\text{cm}^{-2}$ at midgap to $3.5{\cdot}10^{-11}\text{cm}^{-2}$ at $E = 0.7$ eV. The parabolic shape is based on a realistic traps-energy distribution, as for instance reported in [53]. The acquired number of interface states is then randomized using a Poisson pseudo-random number generator, converted into density and assigned to the sub-region. This process is independently repeated until random interface states have been assigned to all the sub-regions along the channel.

2.2.3 Random Series Resistance

A final cause of mismatch that has been implemented and tested in SiSPET is indicated as random series resistance fluctuation. Recently, series resistance fluctuations have been studied in case of advanced device architectures such as FinFET, where the access resistance of the source and drain terminals heavily

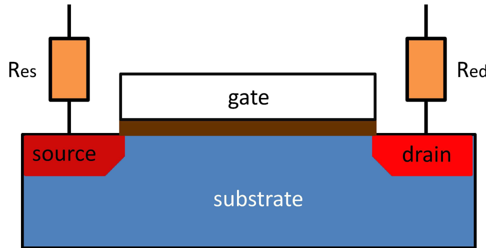


Figure 2.8: Schematic representation of the device structure including the external series resistance added to drain and source terminals.

impacted the mismatch behavior [54, 55]. A similar effect can be observed in bulk MOS or, actually, in any other active device, when the whole device-interconnection system is affected by external (to the device) resistance fluctuations. In case of mismatch measurements, for instance, the external resistance can come from deteriorated probe-to-pad contact while in case of circuits they can come from asymmetric interconnections. In other words, the addition of series resistance fluctuations is meant to verify the influence of external perturbation to the system as a whole. The implementation of RSR in SiSPET is quite straightforward. Two lumped resistors of random value are added in the electrode definition (of source and drain) of the simulator. In figure 2.8 an idealization of the simulated device is depicted. Series resistors are added to source and drain terminals, their values, R_{es} and R_{ed}, are independently and randomly extracted from a uniform probability density function. The uniform distribution has been chosen especially to mimic the behavior of probe-to-pad resistance fluctuations during automatic probed measurements. To substantiate this choice some measurements have been performed. A schematic of the measurement test structure is shown in figure 2.9. It is a structure with a series of short-circuited pads, it is usually used to check if a probe card has been installed and landed on the wafer correctly. For this particular experiment four needles were used: the internal ones (2 and 3 in figure 2.9) are used to force a current into the pads, while all four needles are used to sense a voltage. Since the voltages at needles 1 and 4 are measured 'currentless' the probe-to-pad resistances are obtained with the equations:

$$R_2 = -\frac{V_{\mathrm{SH}} - V_{\mathrm{H}}}{I_{\mathrm{F}}} \tag{2.2}$$

$$R_3 = -\frac{V_{\mathrm{SL}} - V_{\mathrm{L}}}{I_{\mathrm{F}}} \tag{2.3}$$

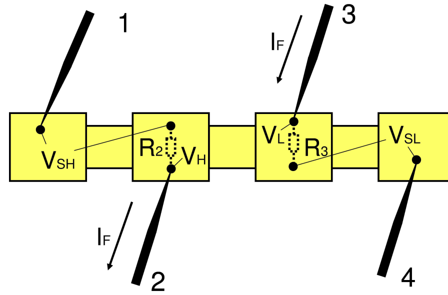


Figure 2.9: Schematic of the test structure for probe-to-pad resistance measurements.

where R_2 (R_3) is the probe-to-pad resistance of needle 2 (3), I_F is the forced current and V_SH and V_H (V_SL and V_L) are the voltages measured at needles 1 and 2 (4 and 3) respectively. These measurements have been performed on 180 positions on a 200-mm wafer with a semi-automatic wafer prober. This is exactly the same procedure as employed for standard mismatch measurements. Some typical results are shown in figure 2.10. In particular, two different behaviors have been selected as examples of what can be considered a 'good' and a 'poor' contact. In case of a good contact the distribution looks gaussian and also all the measured resistances form a narrow distribution. On the other hand, when a probe-to-pad contact shows a high resistance (this happened especially after the pads were deteriorated with multiple landings) the distribution is far from being Gaussian. The resistance varies substantially from 0.4 up to 2.5 Ω. A uniform distribution was chosen for the implementation of RSR in the simulator. In this case a log-normal distribution would have probably done the job as well. The point is however, that there is no reliable estimate for contact resistance in our type of experiments. It varies from experiment to experiment and it depends on pad contamination, sharpness of the needles, aluminum residues sticking to the needles and so on. A uniform probability density function has the advantages to be easy to implement, it will avoid negative numbers but it will overestimate the long tail of the 'poor' contact. RSR was added to the simulations only when the original measurements showed some unexpected results imputable to large probe-to-pad resistance fluctuations (see chapter 4). The range of the uniform distribution is fitted to drain current mismatch measurements. Note that, as it is for RIF also for RSR the aim is to study and understand the qualitative effect rather than using it as a method to extract quantitative information.

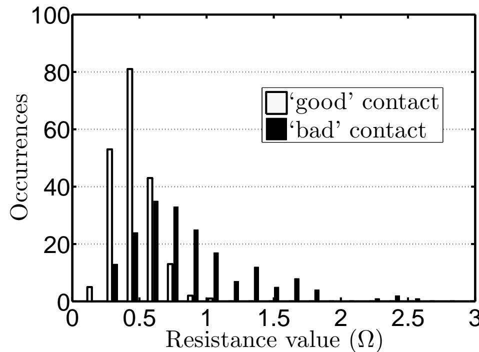


Figure 2.10: Distribution of probe-to-pad resistances measured on 180 different positions. Especially in case of high resistance value ('poor' contact), the distribution is non-gaussian.

2.3 TCAD calibration

Beside the choice and the implementation of these sources of mismatch, a crucial factor for the understanding of the mismatch behavior is the availability of a virtual virgin (unperturbed) device that resembles in the best possible way the actual measured device. A modern MOSFET consists of a quite complex architecture and doping profile. Good confidence in results from device simulations can be attained only when the virtual device is a "fair" copy of the ones actually fabricated[1]. This is a crucial step especially if the goal of the simulations is a better understanding of the mismatch dynamics in contemporary technology nodes. In general, the process of recreating the actual device with TCAD tools is called *TCAD calibration*. Basically, it consists of tuning device construction (either adjusting parameters in a process simulator or in a structure editor) and simulation model parameters until an acceptable level of agreement between simulated and measured electrical performance is reached for all the geometries and bias conditions under test. This task becomes particularly challenging when the device is drawn from scratch, even when the architecture is based on common scaling principles and inputs from the ITRS roadmap [56]. Quite often, detailed process parameters are unknown as they are considered trade secrets. This is for instance the case when the silicon is obtained from external foundries. In this section methodologies and

[1]Of course, the target here is to obtain a very close resemblance to the **median** of a population of measured devices.

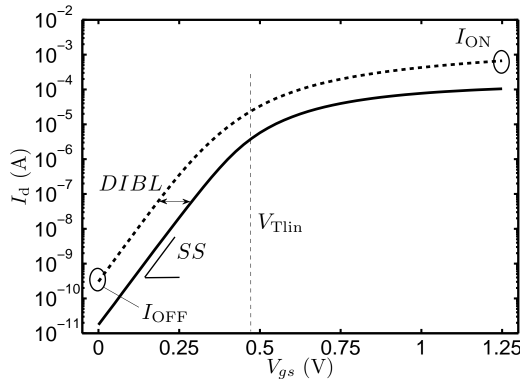


Figure 2.11: Representation of the indicators used for the TCAD calibration on the two drain current curves. The solid and dashed curves represent the drain current obtained with low and high drain voltage respectively.

techniques for such "blind" calibrations are discussed. Furthermore, due to the complicated doping profile that are typical for contemporary MOSFETs (and all the degrees of freedom of a simulator), targeting only parameters such as maximum current delivered, I_{ON}, threshold voltage, V_{T}, leakage current, I_{OFF}, drain induced barrier lowering, $DIBL$, and subthreshold slope, SS, as it is usually done, might not be sufficient. In fact, such a calibration can result in good agreement even with a doping profile far from the reality. This is an undesired situation because second order effects and peculiar mismatch behavior, for which TCAD is such a powerful investigation tool, may not be captured properly. An excellent way to verify the simulated device's doping profile is to evaluate the device behavior as a function of the substrate bias. The presence of halos (high tilt implants to improve short-channel behavior) for instance, makes the doping below the gate non-uniform in the lateral direction. When a substrate bias is applied, the depletion region below the gate will change. Thus, if the doping profile is wrong, it will have a different impact on the threshold voltage compared to measurements.

As explained, the device structure is created directly with SSE. Once the structure has been created (based on ITRS roadmap guidelines [56]) and the initial simulation performed, a comparison with measurements takes place. The classical and simple method consists of comparing the simulations with the measured current in the linear region (low drain voltage) and in the saturation regime (high drain voltage) first for long devices and then going down to the minimum dimensions [57]. The main performance indicators of MOS devices,

such as I_{ON}, I_{OFF}, V_{T}, $DIBL$ and SS, can be determined using these two curves as shown in figure 2.11. Once the measurement data have been collected, the real calibration begins. The simulator and the structure editor offer many adjustable variables and tunable parameters. Some of the main variables are:

- **Doping profiles** are obviously the most important device construction elements, as they play a role in any region of the device characteristic. In modern technologies, due to the presence of halos and composite well implant, there are many degrees of freedom (e.g., concentration and decay gradient).

- **Oxide thickness** and its **dielectric constant** predominantly affect the subthreshold slope and the current factor. The exact values of the thickness and the dielectric constant are often unknown. In modern technology the dielectric is slightly nitrided to reduce leakage and to increase the relative dielectric constant ϵ_{r}.

- Drain and source **extension overlaps** determine how far drain and source extend beneath the gate and hence determine the $DIBL$ and the actual current factor.

- **Gate work function** adjustments are used to shift the curve in one or the other direction to get the correct threshold voltage.

- **Mobility model** parameters play an essential role in determining the current in strong inversion.

Of these five "knobs", the mobility model requires a more detailed discussion. In most of the commercial device simulators there is a wide range of mobility models to choose from. The total effective mobility is the result of a combination of different physical effects, i.e. the mobility reduction due to high doping, degradation at interface due to electric field perpendicular to the carrier direction or the velocity saturation. Moreover, for each effect there are different formulations originating from different studies and approaches. Once the effects that need to be taken into account are selected, the user must choose from the different formulations. Finally, the simulator calculates the overall mobility by adding the different mobility effects following Mathiessen‘s rule [36]:

$$\frac{1}{\mu_{\mathrm{tot}}} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \cdots \tag{2.4}$$

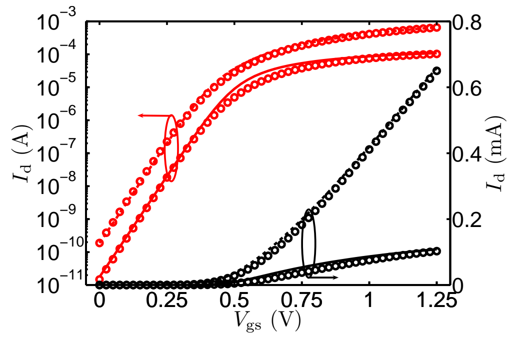
where μ_{tot} is the total mobility and $\mu_{1,\ 2\ \ldots}$ are the different mobility effects that are taken into account. In general, through modifying different sub-models of

the overall mobility, the user can affect the current under a particular bias condition while having a negligible effect on the others. For example the `high field saturation model` will mainly affect the current for high drain bias while the `mobility degradation at the interface` model will predominantly affect the current at low drain bias in long devices. Obviously, all parameters and variables must be kept identical for all the dimensions that will be considered during the analysis. The mobility models used for the simulations reported in this thesis are the Philips Unified Mobility [48] model for the doping dependency (`PhuMob` in SD), the mobility degradation at interface in the formulation proposed in [58] (`Enormal` in SD) and a high field saturation model as formulated in [59] (`HighFieldSaturation` in SD). The fitting parameters of these models were adjusted to match the measured currents. Furthermore, given the small dimensions of the transistor (60-nm gate length) a quantization model for the correct calculation of the carrier distribution was needed. The modified local density approximation (`MLDA` in SD) was chosen as quantization model because of its speed and computational robustness [60].

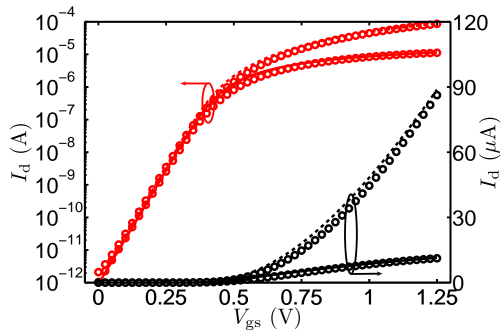
2.3.1 Example of experimental setup and calibration procedure

The technology that needs to be reproduced in simulations, for this calibration example, is a 65-nm Low Power bulk CMOS processed by TSMC [61]. The reference for the calibration was based on the median I-V characteristics of populations of 119 standard V_{T} N-type MOSFETs measured over a 300-mm wafer at 25 °C. Two gate lengths are used for the calibration, namely $L = 1\ \mu$m and 0.06 μm with fixed width $W = 1\ \mu$m.

The first characteristic that one should look at, once a structure with a plausible doping profile is created, is the subthreshold slope. Since the SS is mainly determined by the ratio between the gate and the depletion capacitances it is not influenced by the mobility. It can be modified by tuning the doping profile (especially on the upper region below the oxide) and the gate capacitance (i.e. changing thickness and dielectric constant of the oxide). The next step is the fine tuning of the drain and source overlaps to obtain a $DIBL$ close to the measured value, for the short device. Once the $DIBL$ is correct, the gate work function can be slightly modified to force the simulated curves and the measurements on top of each other in the subthreshold region hence getting the threshold voltage right. Finally, the mobility parameters can be modified to get the right current value in the 'ON' condition. The full procedure may require several iterations of tuning and refining because many of these parameters are correlated. For example, the same $DIBL$ value can be obtained with



(a)



(b)

Figure 2.12: Median drain currents of measurements (symbols) and simulations (lines) in linear and logarithmic scale for two drain-source biases, 50 mV and 1.2 V (solid and dashed lines) and short (a) and long (b) transistor.

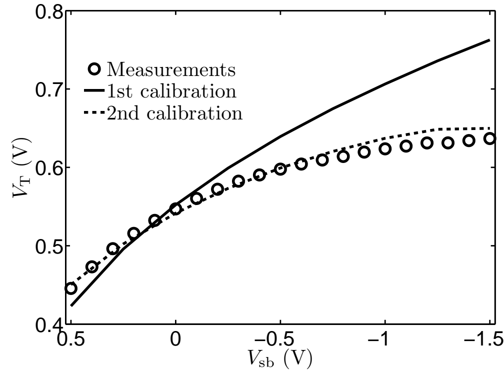


Figure 2.13: Threshold voltage versus body bias for measurements and simulations. The threshold voltage for the first calibration (solid line) keeps increasing more rapidly than the measurements (symbols). After the second calibration the threshold voltage variations with body bias are well captured.

high channel doping and large overlap or with low doping and small overlap. Figure 2.12 shows the result of the calibration procedure sketched above. After proper calibration, the indicators used as reference should all be within ±5% compared to the median measurement.

2.3.2 Body effect

The correlation between the calibration factors also leads to another problem. It proves possible that the device obtained in this way is actually quite far from the reality. A good way to check whether there is a difference between the virtual doping profile and the real one is assessing the body effect, i.e., the dependence of the threshold voltage on the source-substrate bias. Elementary MOS transistor theory predicts that V_T goes with $\sqrt{V_{sb} + 2\phi}$ for uniform substrate doping [62]. The body effect is dependent on the doping in the substrate. The threshold voltage changes accordingly with the movement of the depletion region in the channel region. Figure 2.13 shows V_T for the short device versus the source-substrate bias. For negative substrate biases the measured V_T tends to saturate whereas applying the same bias conditions at the simulated device the threshold voltage keeps increasing with the decreasing of source-substrate bias (red solid line in figure 2.13). This example shows that the device calibrated previously (first calibration) is a clear case of a sub-optimal calibration that met all normally considered observables but failed to follow the body effect

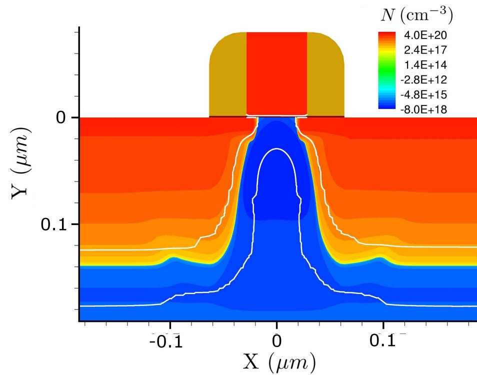


Figure 2.14: Cross-section of simulated device with substrate bias of -1.5V and gate bias of 1.2V, first calibration. The white lines represent the limits of the depletion region. Deep in the channel, the depletion regions coming from drain and source are well separated.

of the actual transistor.

Figure 2.14 depicts the cross-section of the simulated device obtained after the first calibration. The depletion regions from drain and source stay apart even after applying negative source-substrate biases. This causes the discrepancy between measurements and simulations. The depletion regions have still room to extend below the gate resulting in the relatively big impact on the threshold voltage at any change of the back bias. On the other hand, when the dopant concentration underneath the gate is substantially decreased, the depletion layer extends all the way into the lower doped region of the substrate. Consequently, the threshold voltage becomes nearly independent from further decreases of substrate bias. Figure 2.15 shows a cross-section of a device with new doping profile under the same bias conditions. This device has been constructed by lowering the peak values of the halos and of the anti-punch-through implants. The original profiles had too high doping values preventing the depletion regions from penetrating the region between source and drain. With the new doping profile the body effect seen in the measurements is reproduced very well (dashed line in figure 2.13).

For the long devices, measurements and simulations matched very satisfactorily even after the first calibration. The body effect has no such saturation effect. Since the body effect proved to be very useful to check the overall calibration, it is suggested to use it in the early stage of the calibration to extract information about the doping. For example, a simulated V_{T} that varies faster

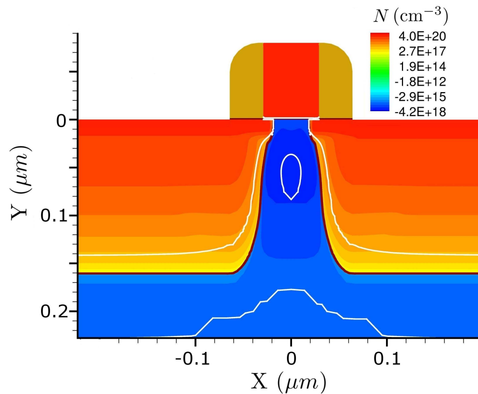


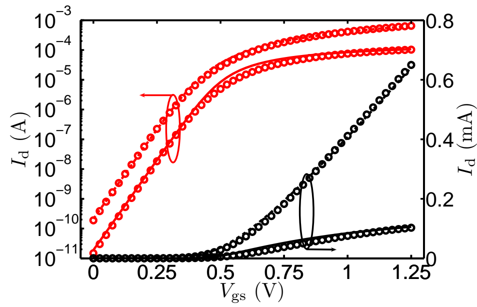
Figure 2.15: Cross-section of simulated device with substrate bias of -1.5V and gate bias of 1.2V, second calibration. The white lines represent the limits of the depletion region. Deep in the channel, the depletion regions coming from drain and source touch.

than measurements in function of V_{sb} may indicate a too high doping or if it saturates earlier it can point towards a too shallow profile. A drawback of this strategy is the simulation time consumption. As a matter of fact, to check the body effect, at least nine additional simulated curves were required, which resulted in a simulation time about five times longer. In the early phase of a calibration such long simulation is not desired considering also that it must be repeated a number of times to reach a decent agreement. However, good back bias behavior guarantees a high level of confidence in the calibration and it is therefore strongly recommended.

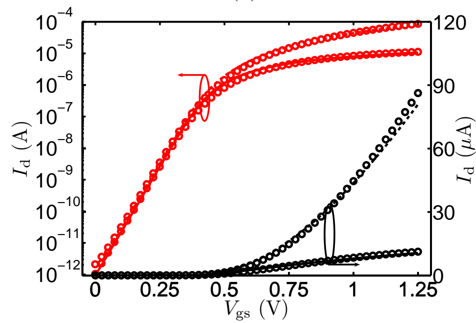
After the correct substrate behavior has been obtained all the calibration steps have to be done again as described in section 2.3.1. The agreement is even better after the second calibration shown in figure 2.16. All the indicators stay within $\pm5\%$ from the target value and the correspondence in moderate inversion even improved.

2.4 Mismatch analysis methodology

Proper determination of statistical estimators and interpretation of subtle mismatches signatures form the real challenge of parametric mismatch characterization for mixed-signal technologies. Thus, a reliable and consistent analysis



(a)



(b)

Figure 2.16: Median drain currents of measurements (symbols) and simulations (lines) in linear and logarithmic scale for both drain-source biases, 50 mV and 1.2 V and short (a) and long (b) transistor after the second calibration. The overall results is slightly better than the first calibration (especially in moderate inversion region).

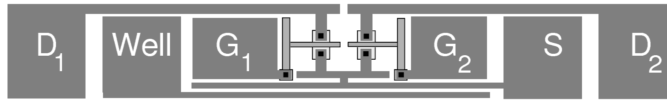


Figure 2.17: Top-view of the pad-based test structure used for MOSFET mismatch characterization [65]. This type of structure allows the measurement of only the random component of mismatch excluding the parametric gradient.

methodology must be used throughout the whole study.

Generally speaking, a parametric mismatch analysis, consists of the evaluation of the difference between two supposedly identical instances, e.g. transistors, resistors etc., repeated on many samples in order to create a population that can provide statistically meaningful estimators. In case of measurements this can be achieved by using a large array, or by spreading single matched pairs over a full wafer in as many dies as possible. The fabrication process of silicon wafers inevitably results in device performance variations across a wafer (parametric gradients or inter die variations). By placing two transistors of a pair close together, the impact of the parametric gradient is mitigated and their difference (of a population of pairs) is dominated by random variations. For devices measured in this thesis, the single pair approach has always been used. A top-view of the layout of a perfectly symmetrical pad-based matched pair test structure used for MOSFET is shown in figure 2.17. The higher flexibility and the simplicity of the design united to the possibility of performing accurate and extensive device measurements offered by single pair approach were preferred to the better statistics offered by an array based structure (for a detailed discussion on characterization methods see [63, 64]).

In case of simulations there is no need to create matched pairs since the perturbed devices are not affected by systematic variation. Therefore, each device of the population, which size will be the result of a trade off between computational time used for the device simulation and acceptable statistical uncertainty, will be compared with the median device of the population. Hence, there will be a factor of $\sqrt{2}$ of difference between the results of simulations and measurements. Unless differently specified, in the remainder of this thesis all the simulation results have been multiplied by this factor for a fair comparison with the measurements.

Our mismatch data analysis can be separated into two main parts. One is the analysis of the mismatch of transistor parameters such as threshold voltage, V_{T}, and current factor, β, usually checking their linearity versus the square root of the active area of the transistor (also known as Pelgrom plot [2]). The

other one is the analysis of the so-called **mismatch signature** that allows evaluation of the relative drain current mismatch in the whole operating range. However, none of these ways is perfect on its own. The extraction of the area factor for threshold voltage and current factor, for example, can give a simple and good comparison with other technologies. The area factor still forms the standard way of implementing mismatch into the design and simulation of most analog circuit blocks but hardly highlights subtle unexpected or undesired device behavior characteristics visible, on the other hand, with the mismatch signature. Thus, these two methods will be mostly used together.

2.4.1 Parameter extraction

It is important to establish a reliable procedure for extracting and analyzing transistor parameters. Croon *et al.* [30] reported different extraction methods for the transistor parameters. In view of their conclusions the three-point extraction method with fixed-gate overdrive also described in [66] was selected as preferred method. The three points method measures the drain currents (I_{d1}, I_{d2} and I_{d3}) at three different gate biases (V_{gs1}, V_{gs2} and V_{gs3}) from which the threshold voltage, V_{T}, the current factor, β, and the mobility reduction factor, θ, are analytically derived [66]. Due to the very simple model, the resulting parameters are dependent on the three measurement points. Using the fixed overdrive method ensures that the bias points have appropriate values, even when the threshold voltage is not, a priori, known. The initial threshold voltage V_{Tin}, is usually determined by a different method (e.g. maximum slope method or current criterion). Our implementation of the three points technique uses iterations, where the calculated V_{T} is used as V_{Tin} for the next iteration cycle. The procedure is repeated several times, typically about 10, until convergence is reached, i.e., the new value does not change by more than 1 mV. The ideal extraction technique does not exist and all methods have their advantages and disadvantages. However, the three point extraction with fixed overdrive seems the most robust against external disturbances like, for instance, series resistance fluctuations (in most cases captured by θ).

2.4.2 Mismatch signature

A closer look at the exact behavior of the relative drain current mismatch behavior over the whole range of operation is necessary when a deeper understanding of the mismatch sources is required. Furthermore, evaluating the mismatch performance of a technology considering only few key numbers, e.g. the area factors of different parameters, can overlook unexpected behavior po-

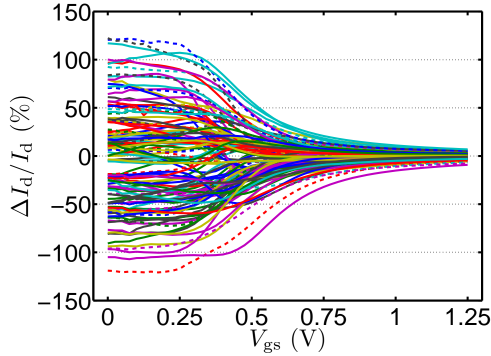


Figure 2.18: The relative drain current mismatch of matched pairs versus gate bias (at $V_{\mathrm{ds}} = 0.05$ V and $V_{\mathrm{bs}} = 0$ V). This figure is further referred to as "mismatch sweeps".

tentially harmful for the electronic building block's performance. Nowadays, the transistors are used more and more in the region around the threshold voltage in order to consume less power. Quite often, though, the simplicity of the mismatch models does not allow a correct description of the device operating in that region. Therefore, it is worthwhile to look at how the mismatch behavior of a device population (or in some cases of an individual matched pair) changes as a function of the operating regimes. The mismatch signature helps the analysis in that sense. It consists of two main elements: **fluctuation sweep** and **auto correlation plot**.

The starting point is the measurement (or the simulation) of relative drain current mismatch between the two transistors of a matched pair (or between the median device and a perturbed one). Let us consider now the case of measurements on a population of 119 matched pairs of n-type MOSFET with a width of 1 μm and a gate length of 0.06 μm fabricated in a 65-nm CMOS technology. In figure 2.18 a full population of relative drain current mismatch measurements is shown. Every curve is an individual measurement performed on a matched pair and shows how the relative current mismatch depends on the V_{gs} for a particular pair. Note that mismatch varies dramatically from pair to pair, but also note that there are pairs where the mismatch is negative for low V_{gs} while it turns positive for higher V_{gs} and vice versa. The collection of mismatch sweeps can be compacted into two curves that are called **mismatch signature**. The first is the so-called fluctuation sweep (see figure 2.19), where the standard deviation of the relative drain current mismatch for the full pop-

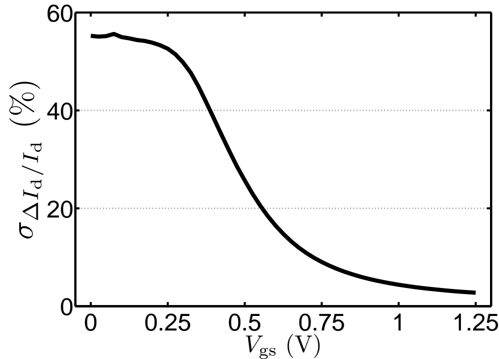


Figure 2.19: The standard deviation of the relative drain current mismatch of the whole population versus the applied gate-source voltage (same data as in figure 2.18). This figure is further referred to as "fluctuation sweep".

ulation is plotted versus gate voltage (in symbols: $\sigma_{\Delta I_\mathrm{d}/I_\mathrm{d}}$ vs. V_gs). This curve gives an indication on how the transistor mismatch standard deviation changes with the gate voltage over the full operation region. The second curve is the autocorrelation plot (see figure 2.20). It consists of the autocorrelation coefficient between the relative drain current mismatch at any gate bias and the one observed at threshold voltage, in symbols: $\rho^2(\Delta I_\mathrm{d}/I_\mathrm{d}(V_\mathrm{gs}), \Delta I_\mathrm{d}/I_\mathrm{d}(V_\mathrm{T}))$ vs V_gs. The autocorrelation plot reveals something about the mismatch mechanisms that influence the transistor behavior. In case of MOSFET, the threshold voltage is chosen as reference. Because the majority of threshold voltage mismatch is caused by random doping fluctuations, any diminution of correlation is an indication of a possibly different, more precisely independent, mechanism that significantly affects the mismatch in the other regions of operation. An attempt to understand the causes of mismatch governing the subthreshold region is described in chapter 3. An extreme de-correlation in the strong inversion region in a Lateral Diffused MOS mismatch measurement will be treated in chapter 4.

2.5 Summary

In this chapter the simulation approach and analysis methodology used throughout this thesis have been described. The advantage of having a tool capable of simulating sources of fluctuations for process technology already in production has been explained. The statistical simulations will be based on 2-D

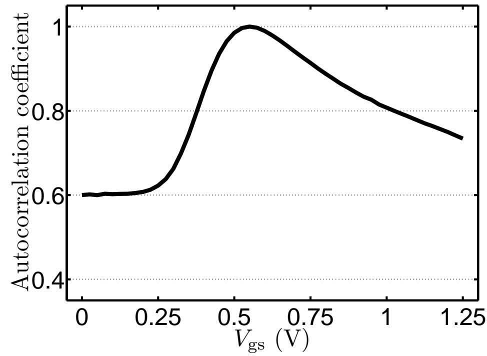


Figure 2.20: The autocorrelation coefficient between the relative drain current mismatch at any gate bias and the mismatch at $V_{\mathrm{gs}} = V_{\mathrm{T}}$ of the whole population (same data as in figure 2.18). This figure is further referred to as "autocorrelation plot".

simulations with a relatively large virtual width such that the resulting device with fluctuations (especially when RDF are considered) will not suffer from large and abrupt doping variations. Furthermore, some guidelines for a standard TCAD calibration with the help of the substrate voltage dependence have been discussed. In the last part of the chapter the analysis methodology used throughout the thesis has been introduced.

Chapter 3

Interface state fluctuations

This chapter treats the impact of interface states fluctuations on MOS transistor mismatch. Based on modified 2-D drift-diffusion device simulations, mismatch signatures and principal component analysis, interface state fluctuations are shown to cause a significant contribution to mismatch. Subsequently, our findings are challenged by trying different ways to simulate interface state fluctuations and to isolate their effect in dedicated very-fast pulsed I-V measurements. Furthermore, first steps towards the implementation of the possible impact of interface states in a compact model are made.

The outline of this chapter is as follows: first the identification of interface state fluctuations as second major contributor to mismatch after random dopant fluctuations in contemporary n-channel MOSFETs is explained. Then the simulation methodology and its results are described. After incorporating the impact of interface states in a compact model, the different results obtained with a different simulation methodology are illustrated. The last part of the chapter is about the experiment of measuring with very-fast pulsed I-V equipment in order to separate possible effect of slow interface states from the mismatch behavior. Conclusions and recommendation for future work are given in the last section.

3.1 Interface states and mismatch signature

Traditionally, random dopant fluctuations have been considered the most important cause of mismatch (and extensively studied) since the beginning of this

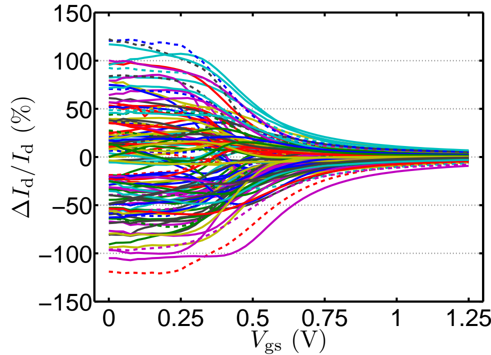


Figure 3.1: An example of measured mismatch sweeps of 1/0.06 μm/μm NMOS matched pairs.

research topic [1, 21, 2, 6, 12, 41]. On the other hand, other sources of mismatch have not received much attention until only a few years back. This was probably not necessary in the past when simpler device architectures and large gate bias overdrives made life a little bit easier for circuit designers. Models and analysis based on an RDF-only theory proved sufficiently accurate to describe the mismatch properties.

Nowadays, both the shrinking of the devices and changes in the architecture (e.g., SOI and FinFet) require a more thorough investigation of other possible sources of mismatch. Among them, poly-silicon granularity [28, 31], line edge roughness [67, 15] and fixed oxide charges [52] are the ones that recently attracted the most attention.

Although interface states have been a major concern for the MOSFET-based semiconductor industry from the start (initially it was impossible to fabricate a functional MOS transistor because of a too contaminated interface) and their fluctuations was a point of concern from the point of variability many years ago [51], this worry has largely faded away. Interface state and oxide charge fluctuations are the most plausible cause for 1/f noise and many stress-induced instabilities [68, 69]. Nevertheless their influence on the mismatch behavior of MOS transistor has not been thoroughly treated. Through simulations and dedicated measurements the investigation illustrated in this chapter will fill this gap.

Let us take as example the mismatch sweeps of a measured population of NMOS matched pair transistor fabricated in 65-nm node technology (C65) as shown in figure 2.18 in chapter 2 and replicated here for convenience in

figure 3.1. The mismatch sweeps of well-calibrated transistors of the same gate length obtained with RDF-only simulations (as explained in section 2.2.1) are shown in figure 3.2. For the simulated results the size of the population is 51 and the mismatch is calculated by comparing each simulated device with the median of the population. The mismatch for each simulated device is then multiplied by $\sqrt{2} \cdot \sqrt{10}$. The factor $\sqrt{2}$ compensates for the fact that the mismatch is calculated using the median as reference and not using matched pairs while the $\sqrt{10}$ normalizes the results to 1-μm width (note that 10-μm wide devices are simulated, see section 2.2.1). The latest normalization is done following the classical area scaling rule formulated in [2, 70] and shown in chapter 1 as well. By doing so it is implicitly assumed that the area scaling holds for these devices. This is allowed as the conditions required by Pelgrom's derivation based on the central-limit theorem are met for these small perturbations. The choice of simulating very large transistors implies that this 2-D simulator approach is representative for relatively wide bulk devices that are not severely affected by narrow width effects. For a fair comparison though, also the measurement data presented in this thesis were obtained from device populations that meet this assumption.

Besides the substantial difference in magnitude between measured and simulated populations, one can also notice remarkably different shapes. In the RDF-only simulation case, in fact, the various $\Delta I_{\mathrm{d}}/I_{\mathrm{d}}$ are in subthreshold almost all parallel and hardly cross each other (see figure 3.2) whilst the measured curves show the tendency of crossing-over and even changing sign when sweeping the gate voltage.

From the mismatch sweeps, the mismatch signatures (figures 3.3 and 3.4) can be calculated. Two macroscopic differences are visible in the comparison of the signatures.

In the first place, the magnitude of the simulated standard deviation is equal to the measured one in strong inversion but almost half in subthreshold. Second, also the autocorrelation plots show a good agreement in strong inversion whereas there is a big difference below threshold. These observations led to the following conclusions.

Apparently, our approach for RDF simulations, based on the inclusion of the mobility models in the simulations, yields a very good agreement for the drain current fluctuation in the strong inversion region. It is widely recognized that the relative drain current mismatch of a MOSFET in strong inversion is mainly determined by the relative current factor mismatch (β) which, in turn, is predominantly attributed to the mobility mismatch. This means that the large majority of the drain current mismatch in **strong inversion** is explained by RDF. It appears therefore that the consequences of RDF, both doping level

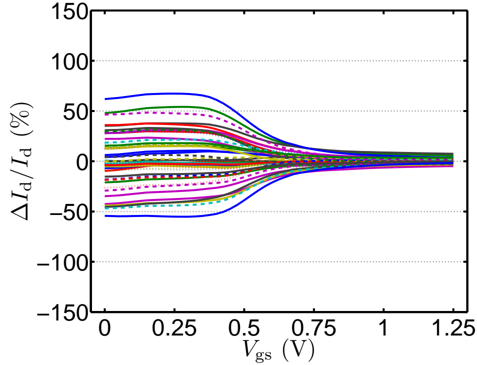


Figure 3.2: Mismatch sweeps of 10/0.06 μm/μm 51 NMOS transistors as obtained using RDF-only simulations. The results are then multiplied by $\sqrt{2}\cdot\sqrt{10}$ for a fair comparison with measurements. Note that the curves remain practically parallel over the complete bias range.

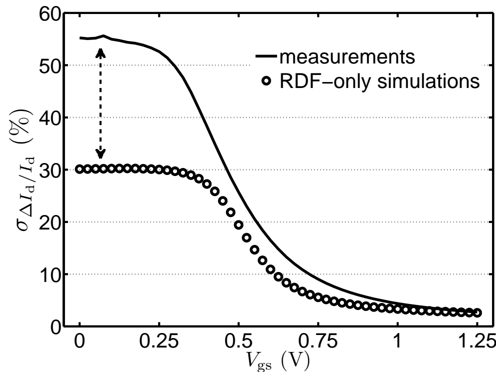


Figure 3.3: Fluctuation sweeps of measurements and RDF-only simulations of 1/0.06 μm/μm NMOS transistors fabricated in C65 technology. The results for simulations are already scaled.

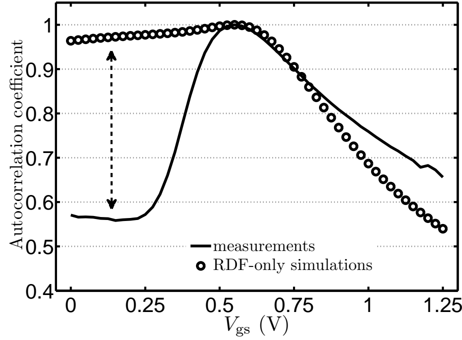


Figure 3.4: Autocorrelation plots of measurements and RDF simulations of 1/0.06 μm/μm NMOS transistors fabricated in C65 technology.

fluctuations and modifications of the electric field, are well captured by the standard mobility models in simulations when the variation of the doping itself is kept in a reasonable range (made possible by using very wide devices) thus to avoid artifacts and unrealistic peaks of electric fields as discussed in chapter 2.

However, using RDF-only simulations the subthreshold part is not well described. The most plausible explanations are two: either the two-dimensional RDF simulator is not capable of simulating subtle, mainly 3-D, effects like percolation[1] [8, 71], or there is another source of mismatch that is important in weak and moderate inversion regions. Since strong percolation effect are not very likely in a 10-μm wide (or even 1-μm wide) devices, it was decided to test the second possibility and to verify whether with our analysis method and simulation capabilities this extra source of mismatch could be isolated.

To separate independent mechanisms contributing to the drain current mismatch a `Principal Component Analysis` (PCA) was applied to the sets of data for both measurements and simulations using the built-in Matlab routine [72].

PCA is a mathematical technique widely used for data analysis of a multivariable system. Through an orthogonal linear transformation, PCA converts a set of observations of possibly correlated variables into a set of uncorrelated variables called *principal components*. The number of components is determined by the size of the given dataset. Every new extracted component is a

[1] Percolation is the flow of electrons through low resistance path in the channel before a complete inversion region is created.

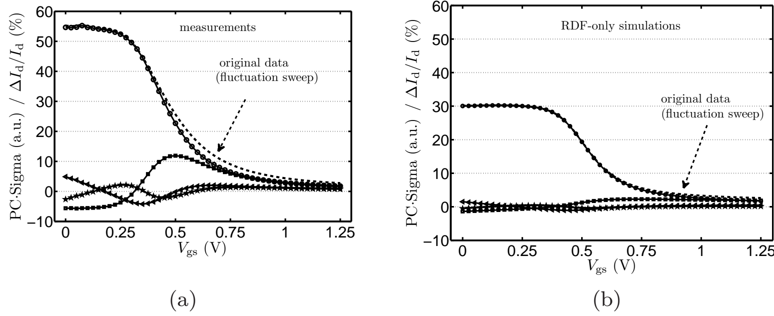


Figure 3.5: Principal component analysis performed on mismatch sweeps obtained from measurements (a) and RDF-only simulations (b). The dashed lines represent the original fluctuation sweeps which are in fact captured exactly (within the resolution of this plot) with the first four principal components.

geometrical base of the data space such that it is orthogonal to all the others already extracted, and the variance of the projection of the data on this base is maximized. All the principal components together represent an orthogonal basis for the space of the data. The goal of PCA is to reduce a complex data set caused by correlated variables into an other much simpler set where few variables cause the large majority of the data variation. By examining plots of these few new variables it is sometimes possible to discover hidden physical causes or, in general, help to corroborate the understanding of the driving forces that generated the original dispersion of the data [72, 73].

This is exactly what was done by applying PCA to our sets of mismatch sweeps. In the figure 3.5 the first four principal components of measurements (a) and simulations (b) with the original fluctuation sweeps (dashed line) are shown. As explained above, PCA provides a number of components equal to the number of available curves (119 and 51 for measurements and simulations respectively). Only the first four, i.e. the most significant four, are plotted here because the original fluctuation is very well reproduced from the combination of these four.

These graphs further substantiate the need for our search for the “hidden” cause of mismatch. In the case of PCA of measurements there clearly is a strong second component that is mainly “active” in weak and moderate inversion while there also is a difference in shape when comparing the fluctuation sweep and the first component. On the other hand, the higher-order components calculated for RDF-only simulations are much weaker and also

already the first component alone almost exactly reproduces the fluctuation sweep. This should not come as a surprise since all the fluctuations, in the simulated case, are the result of a single controlled fluctuation source (RDF), thus all the other orthogonal extracted basis are reduced to the bare minimum. This, in fact, demonstrates that the theory and the implementation of PCA worked well. The PCA therefore reveals that for measurements there must be another uncorrelated source of mismatch that plays a role especially in weak and moderate inversion.

Summarizing: to explain these observations a source of fluctuation is needed that is uncorrelated to random doping, that scales with the square root of the active area and that is mainly effective in weak and moderate inversion region. With these premises, interface state fluctuations seem to be a likely candidate: interface states are, to first approximation, uncorrelated to RDF, their number scales with the area and their main effect is visible when the inversion channel is not completely formed and it is bias dependent as the Fermi level sweeps through the silicon band-gap filling or emptying interface states located at different energies.

3.2 Simulation of interface state fluctuations

In section 2.2.2, our approach to add interface states in user-defined sub-regions (or slices) along the Silicon/Oxide interface with randomized energy and number was introduced. Summarizing: the channel is divided into 2-nm subregions along the channel direction. A number of traps with the same randomly selected energy is assigned for each sub-region. The nominal number of traps is chosen from a realistic distribution. The actual number of interface states assigned to the sub-region is extracted by a Poisson pseudo-random number generator that uses the nominal value as the expected value.

As for the RDF simulations, a large (virtual) device width of 10 μm is used to keep variations of interface states densities relatively small, hence avoiding large abrupt electric field changes enabling the use of drift-diffusion simulations with standard mobility models.

One of the innovative points of this part of the work is the fact that random energies are assigned to the interface states. The effect of randomizing trap energy is easily quantified by a reference calculation, simulating interface state fluctuations with fixed energy (equal to mid-gap). A large value for the nominal density ($2 \cdot 10^{12}$ cm^{-2}) has been chosen for RIF with fixed energy to demonstrate the effect.

Figures 3.6 and 3.7 summarize results obtained for 60-nm long RDF and

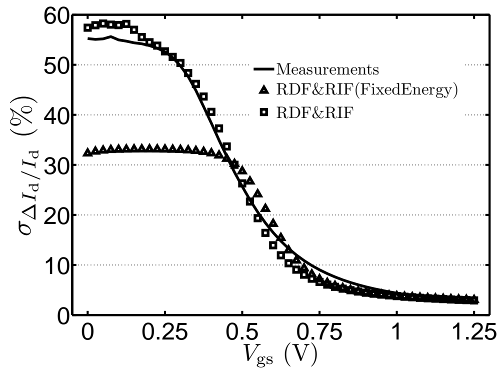


Figure 3.6: Fluctuation sweeps of measured 1/0.06 μm/μm NMOS matched pairs and simulated devices. The fluctuation sweep obtained with simulated results with random energy are very similar to the measurement. In moderate inversion, the simulations and the measurements show still some discrepancies.

RIF perturbed devices. Mismatch signatures of measurements and simulations with random interface state fluctuations (both with random and fixed energy) are shown.

The signature associated with simulations with RIF with fixed energy, even though they were added in a relatively large quantity, resembles in many parts the signature seen with RDF-only simulations. A clear impact can be seen only in the shift of the fluctuation sweep curve towards higher gate bias. This is the result of the increase of the threshold voltage, roughly 60 mV, due to the large quantity of charges added to the interface. The fluctuation sweep below threshold has increased slightly but the correlation coefficient remains close to 1. This is because all states will be charged at sufficiently low gate bias.

On the other hand, the signature of the simulated device population changes completely when adding interface states with random energy (as described in section 2.2.2). The relative current mismatch in subthreshold now reaches the same magnitude as the measurements and the autocorrelation plot is impacted as well, showing a significant amount of de-correlation at low gate bias when compared to the relative drain current mismatch at threshold voltage. Moreover, as expected, the interface states act mainly in weak inversion while in strong inversion the fluctuations (and the correlation) are basically unaltered. This demonstrates that randomizing the interface states energy levels proves essential. Although the signature clearly changes in moderate inversion, the correlation remains fixed once all states are charged at sufficiently low gate bias

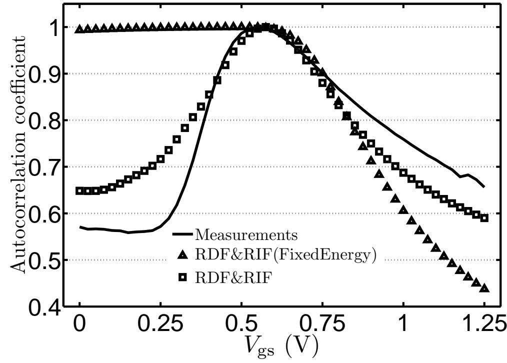
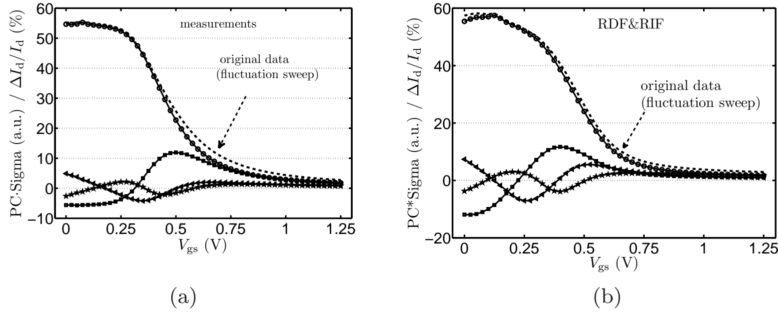


Figure 3.7: Autocorrelation plots of measured 1/0.06 μm/μm NMOS matched pairs and simulated devices. The autocorrelation coefficient for the fixed energy simulations remains very close to 1 in subthreshold.



(a) (b)

Figure 3.8: Principal component analysis performed on mismatch sweeps obtained from measurements (a) and RDF& RIF simulations (b). The dashed lines represent the original fluctuation sweeps which are in fact captured exactly (within the resolution of this plot) with the first four principal components.

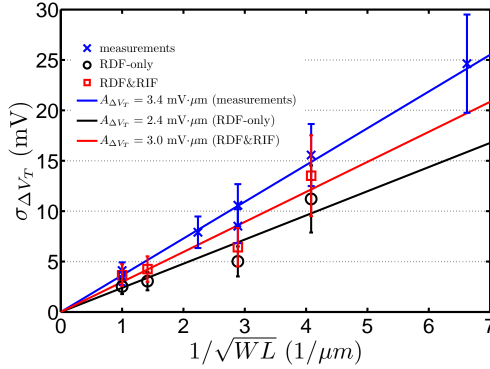


Figure 3.9: Pelgrom's plot of threshold voltage mismatch. For comparison with measurements, all standard deviations are normalized to a device width of 1 μm. Error bars represent the normal 3-sigma statistical uncertainty levels, i.e. $\pm 3\sigma/\sqrt{2(N_{\text{pop}}-1)}$, where N_{pop} is the population size, which is 115 pairs and 51 devices for measurements and simulations respectively.

as is the case for the measurements.

As further confirmation, principal component analyses are applied again to the simulated data obtained with RIF and random energy. In this case, the experimentally observed gate bias dependence of higher order components in the moderate and weak inversion is very well replicated (figure 3.8).

The threshold voltage mismatch area scalings of measurements and simulations are compared in figure 3.9. Error bars are included in this picture and they represent the 3-σ uncertainty associated with the limited population size. The area scaling for simulations has been obtained by simulating four different gate lengths (fixed 10-μm width). For measurements, seven different dimensions were used. The $A_{\Delta V_{\text{T}}}$ associated with the RDF&RIF simulations is certainly closer to the measurements than the RDF-only simulations although the difference still remains significant. This might be attributed to the fact that, as it is possible to see in the fluctuation sweeps (figures 3.6), there are still discrepancies between simulations and measurements in the moderate inversion part, especially close to the threshold voltage. This imperfection is very likely reflected in a moderate impact of the interface states on the threshold voltage mismatch. Probably, a slight modification of the energy distribution of the traps will correct this deviation. However, in view of the available time in the project, this refinement was not pursued.

3.3 Compact modeling of RIF

The final goal of this kind of investigation should always be the improvement of models for circuit designers. Any model improvement means a certain improvement in final result. Therefore, a first attempt to capture RIF in the PSP compact model was made. The compact model chosen for this purpose is PSP [74], the surface potential based model chosen by the semiconductor industry as standard for accurate simulations of MOS devices. The purpose of this attempt is to see whether the present simple implementation of mismatch in PSP is capable to capture the effect of RIF and in case that fails what would be a possible easy to implement solution. The quality of the PSP mismatch implementation is again evaluated through both mismatch sweeps and mismatch signatures.

The PSP model consists of equations that very accurately mimic the transistor behavior. Both the equations and the main parameters associated with them have a strong physical background. With such strong physical base is supposed to be fairly easy to find the most suitable (best fitting) parameter and reason about its impact on the drain current.

Normally, the set of parameters that form the input to a transistor model in a circuit simulator is called model deck. Any technology or device flavor, e.g., thick or thin oxide, high, standard or low threshold voltage, has its own well-calibrated “general” deck and all the dependence of device dimensions and temperature are taken into account through so-called binning and length and width scaling equations for parameters. As this part of the study formed an initial exploration of how to link compact model parameter extraction to SiSPET, only one dimension and one type is analyzed.

The evaluation procedure is as follows. First, a so-called ‘golden’ deck is extracted using the standard procedure as recommended for the PSP model [74] and carefully fitted to the median device of the simulated RDF&RIF perturbed population. For the other perturbed devices an automatic extraction procedure is put in place for the IC-CAP extraction package [35]. Starting from the golden deck only two selections of parameters are allowed to fluctuate for capturing the simulated drain current fluctuations. One set resembles the commonly used approach for modeling MOS transistor mismatch and is composed of only two parameters. These two parameters are in PSP: DPHIB, linked to the threshold voltage, and BETN, a parameter related to the low-field mobility. It is worthwhile to know that these two parameters, during the automatic procedure, are extracted in different regimes of transistor operation: for DPHIB the optimization is done minimizing the difference between the original current and the one calculated with the compact model in *subthreshold* while for BETN only

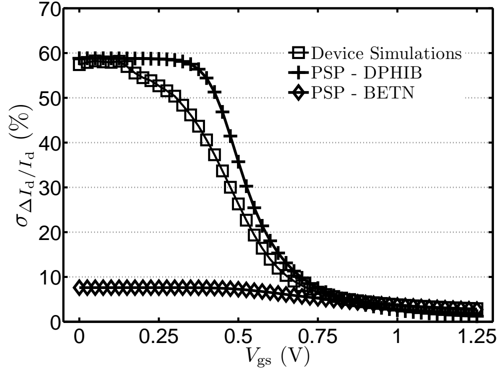


Figure 3.10: Fluctuation sweeps obtained by using only one parameter of PSP at the time. Using DPHIB the agreement between simulations and compact model is good in subthreshold but bad in strong inversion. Using BETN the agreement is good in strong inversion but bad in subthreshold.

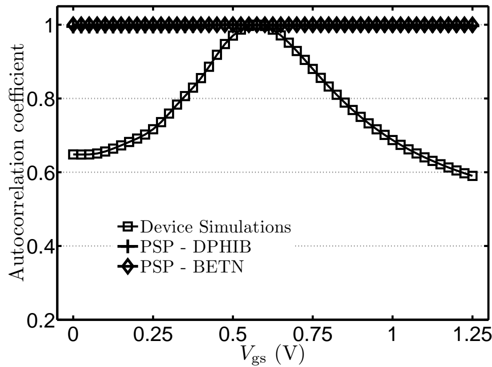


Figure 3.11: Autocorrelation plots obtained by using only one parameter of PSP at the time. In both cases the autocorrelation plot remains close to '1' in subthreshold.

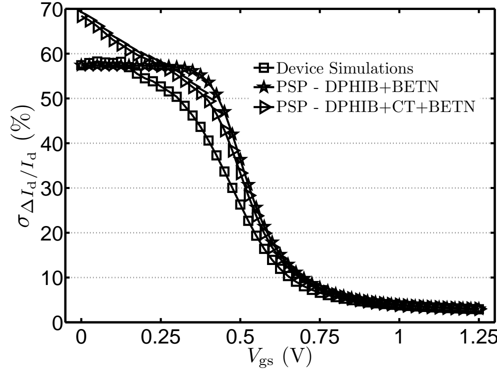


Figure 3.12: Fluctuation sweeps obtained with the two approaches within PSP framework compared to the original simulated data.

the current in *strong inversion* is optimized. This minimizes the correlation between the two parameters[2].

The second approach differs only by the fact that a third parameter, CT, related to interface states is allowed to adapt during the extraction. This parameter affects mainly the subthreshold slope of the device and it is, in fact, extracted modeling the current in subthreshold together with DPHIB.

Subsequently, new drain currents are calculated with the model using the resulting statistics of these parameters.

To further clarify the differences between DPHIB and BETN, figures 3.10 and 3.11 show the mismatch signatures obtained when using only one parameter to reproduce the simulations results in PSP. The fluctuation sweeps show how the two parameters act in two different operation regions of the transistor. The fluctuations of DPHIB are indeed able to reproduce the simulated fluctuations in subthreshold while the fluctuations of BETN improves the agreement in strong inversion. This confirms the need for the two independent parameter to cover the full bias range. The results obtained when the two parameters are put together (as well as when a third parameter is added) are shown in figures 3.12 and 3.13. Although DPHIB and BETN in the two-parameter set are independently fluctuated and the magnitude of the mismatch in subthreshold is quite good, this solution does not replicate the simulated mismatch signature in subthreshold, in particular the autocorrelation plot remains constant and

[2]Note that this approach deviates from a V_T based mismatch assessment using a 3-pt extraction technique. It will more closely resemble a fixed-current V_T extraction technique [30].

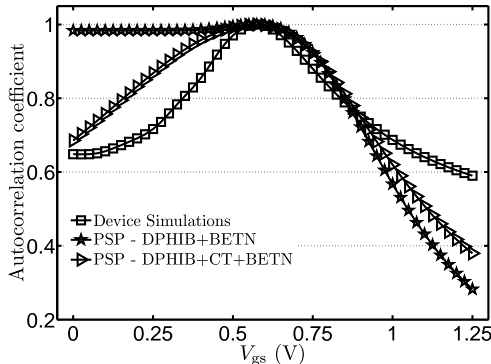


Figure 3.13: Autocorrelation plots obtained with the two approaches within PSP framework compared to the original simulated data.

close to one, below V_T.

With the introduction of CT the de-correlation is much better captured. On the other hand, the fluctuation sweep including CT shows a constant increase of the standard deviation of drain current mismatch when V_{gs} decreases, see figure 3.12. This particular mismatch signature indicates that the subthreshold slope increases at low gate bias, aggravating the impact of threshold voltage fluctuations on the drain current fluctuations. This result demonstrates that the present implementation of the impact of interface states in PSP is not optimized for modeling interface state fluctuations. Further modeling work would therefore be required to solve this shortcoming.

Yet figure 3.14, that combines the mismatch sweeps of the original simulated data and the curves obtained with the two sets of PSP parameters, demonstrates that to describe subtle gate bias dependent mismatch effects in high-precision low-power circuits, an additional component as the one proposed in this study is indispensable. The mismatch sweeps of the two-parameter set shows completely parallel and non-interleaving curves, in contrast with both the experiments, simulations and the three-parameter PSP model results.

In a general sense, this kind of approach, adding an extra fluctuating parameter in subthreshold, is found to be useful also to model very advanced technology nodes. It was shown, in fact, that an independent factor related to the subthreshold slope variability (e.g., line edge roughness) helped to correctly model FinFET mismatch in subthreshold [75].

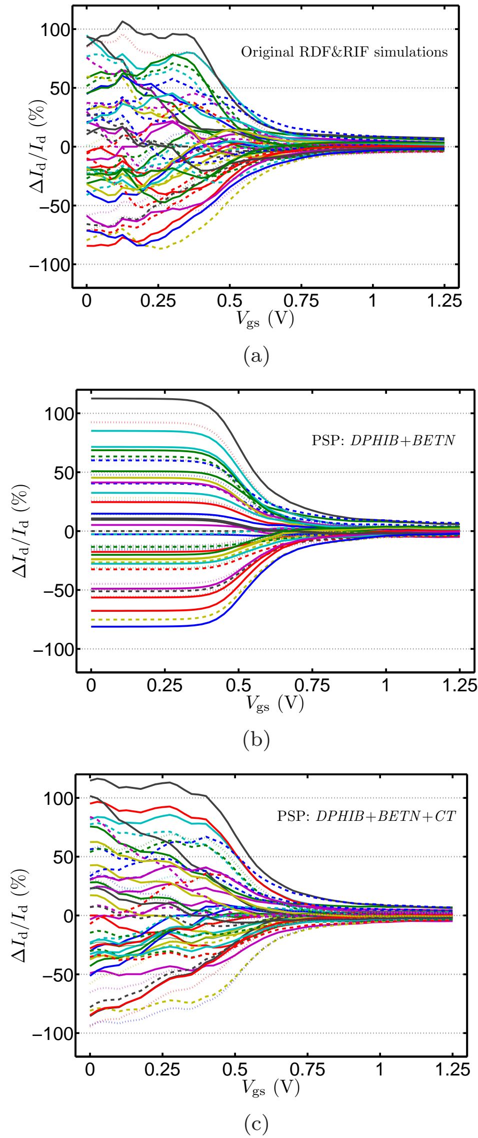


Figure 3.14: Mismatch sweeps of original simulated data (a), drain currents obtained with PSP with two-parameter (b) and three-parameter (c) sets.

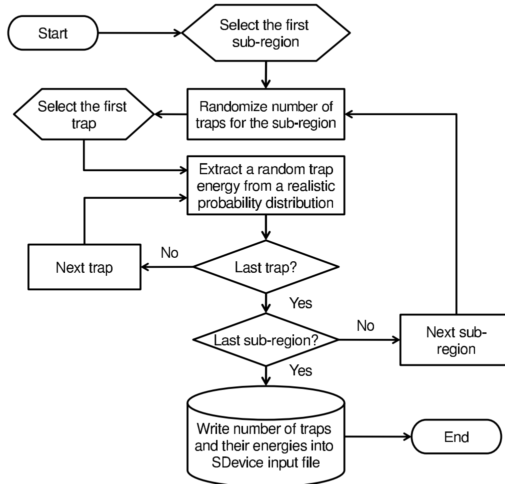


Figure 3.15: Simplified flowchart of the new implementation of interface state fluctuations in SiSPET.

3.4 A discussion on the implementation of RIF

The algorithm used to introduce random interface states in the simulator as described in 2.2.2 contains several simplifications that are in fact not entirely correct. In fact, although the overall energy distribution is globally preserved in the approach discussed so far, assigning only one trap energy per sub-section is a simplified assumption. A different implementation has been therefore tested in SiSPET to study the influence of these settings on the results.

In this algorithm, depicted in figure 3.15, the same channel segmentation is used as before (see section 2.2.2). However, now the number of traps present in the chosen sub-section is randomly extracted (following a Poisson distribution). The mean number is calculated integrating the used energy distribution over the energy spectrum and then dividing the resulting concentration by the area of a sub-region. Then, a random energy is designated to each trap. The typical trap distribution of silicon/oxynitride interface as used for the first implementation serves as the probability density function for the random energy assignment.

The simulated population used for the experiment is exactly the same as the one used for the other implementation of RIF with random energy (section 3.2). However the outcome is remarkably different.

Figures 3.16 and 3.17 show the mismatch signature of these simulations in

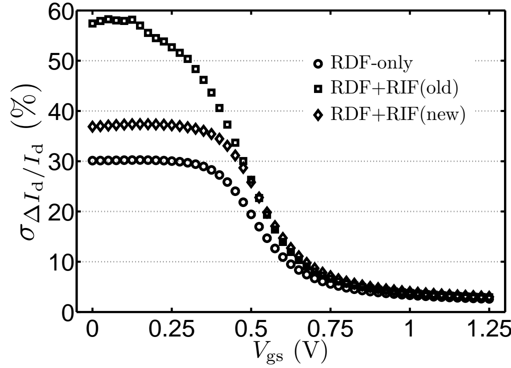


Figure 3.16: Comparison of fluctuation sweeps obtained with simulations of RDF-only and with the two implementations of RIF.

comparison with the earlier reported simulations with and without RIF. The de-correlation effect observed earlier in subthreshold in the fluctuation sweeps of simulated devices with RIF is almost completely gone. The lateral shift of the standard deviation of the drain current mismatch towards higher gate bias is very similar to the one shown for the original RIF. This confirms that the (mean) number of interface states actually present in the devices is basically equal for both implementations.

However, the magnitude of the drain current mismatch below threshold is visibly higher than the RDF-only but still far below the level reached with the original RIF (and consequently the measured level). Basically the same deviating from expected result is obtained with the autocorrelation plot. As depicted in figure 3.17, the level of autocorrelation of the new RIF is remarkably similar to the one of RDF-only simulations.

Further investigation led to the insight that the earlier RIF-implementation was incorrect. It seemed that although the total amount of traps and the energy distribution were good, i.e., using the extracted random number the energy distribution used as nominal/reference could be reproduced, some local fluctuations were affecting the transistor behavior more than expected. In the simulated transistor of 60 nm, the highly doped regions of the halos in the channel overlap in the middle of the channel. As a consequence, the surface potential of these short devices has a valley in the middle of the channel. Although the impact of the fluctuation of this lower point of the potential is not as severe as in long transistors with heavy halo implants [31], the traps in few sub-regions in the middle would control most of the extra-fluctuation brought

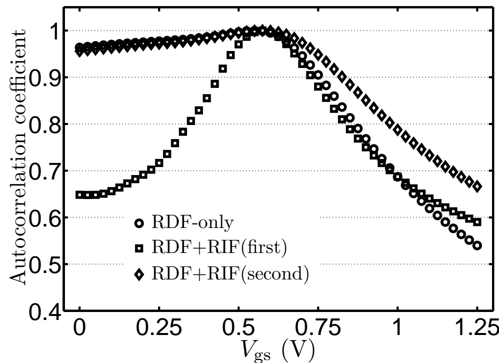


Figure 3.17: Comparison of autocorrelation plots obtained with simulations of RDF-only and with the two implementations of RIF.

in by interface states. Especially in the case of one energy per sub-region, the gate voltages at which the interface state would begin to significantly affect the current flow are determined by the few energies associated with the few sub-regions in the surrounding of the center of the channel. When traps with different energies are assigned to the sub-region this effect is much weaker.

The second implementation is more sound. However, it still suffers from the generic limitation of a 2-D simulator. Especially when analyzing fluctuations that locally have this big effect, a 3-D simulation would be required to reach quantitatively correct predictions. It is possible, in fact, that by assigning the same energy to all the traps in the same sub-region, an artificial barrier for the carriers is created. This will affect the transistor behavior significantly. At the same time, when several energies, that in reality would be found in different position over the width of the device, are all concentrated in the same "2-D" point the overall effect might be mitigated. When considering RDF alone this seemed not to be a problem. Nevertheless, when adding interface states that strongly interact with the surface potential locally in the channel, the 2-D limitation may become an issue, especially in subthreshold.

3.5 Fast pulsed I-V measurements

In order to have a third, independent, way to test the influence of interface state fluctuations on MOS transistor mismatch an experiment that makes use of ultra-fast pulsed I-V measurements was performed. To isolate the effect of

random interface states to transistor mismatch a set of dedicated matching experiments was conducted by using very fast "DC" pulsed I-V measurements pulses. If the reaction time of the traps associated with the observed mismatch degradation in weak inversion is longer than the duration of the pulse, the drain current should be measured without changing the traps' state (empty or filled). This, in turn, will screen the effect of their fluctuation on the surface potential and thus on the mismatch behavior. In other words: if the measurement is fast enough, a possible contribution to the mismatch could be suppressed. This is very similar to other experiments where 1/f noise was shown to be reduced when large slow signal (switched measurements) was applied [76, 77, 78, 79].

Therefore, a thorough comparison between measurements done with standard parametric test equipment (DC) and those obtained through ultra-fast pulsed I-V instrumentation (PMU) is made.

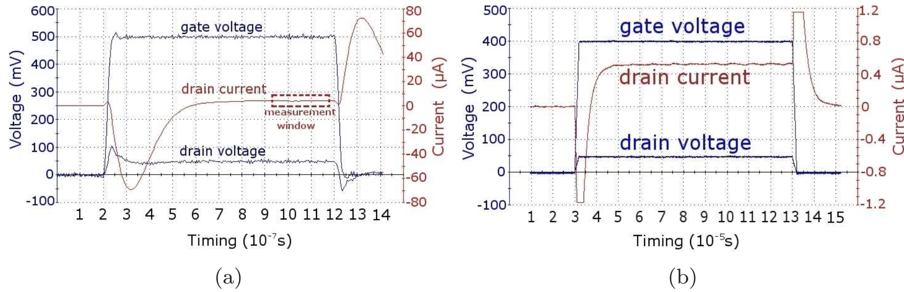
The experiment itself is challenging to any type of measurement instrumentation as the goal is to measure relatively low currents in very short times. The influence of measurement settings, e.g. pulse width and initialization voltage, is analyzed to test the limits of the instrumentation and to have a broader comparison. Furthermore, both standard and pulsed DC mismatch measurements have been performed on hot carrier injection (HCI) stressed devices in which the trap concentration was enhanced.

This section summarizes, in fact, the first successful MOSFET mismatch characterization in the weak and strong inversion regions using microsecond pulsed DC measurements [80].

3.5.1 Experimental setup

This experiment is based on the same C65 technology NMOS devices described earlier in this chapter. Fresh populations of 80 NMOST matched pairs of minimum gate length, $W/L = 1/0.06$ μm/μm are tested. The devices of each pair are measured using a Keithley 4200-SCS, equipped with 4225-PMU ultra-fast I-V instrumentation and 4225-RPM remote amplifier/switches [81]. To the best of our knowledge, this is the only equipment commercially available that allows the type of investigation reported here. Note that the pulses are simultaneously applied to the gate and drain terminals while source and well are grounded.

The objective is to measure the drain current matching of MOSFETs down to the lowest possible current levels using the shortest possible time pulses and compare the results with standard DC measurements. The main region of interest is the weak inversion region, as the impact of the state-switching (charged / uncharged) of interface states occurs predominantly in that regime



(a) (b)

Figure 3.18: Pulse waveforms measured with the PMU as visualized on the 4200-SCS. The pulse widths are 1 μs and 100 μs for (a) and (b) respectively. The part of the pulse where the actual measurement takes place is indicated in (a) by the dashed measurement window.

where the Fermi-level moves through the silicon band-gap.

Examples of the actual pulse shapes, as captured through the 4225-PMU with two different pulse widths (1 μs and 100 μs), are shown in figure 3.18 where the gate and the drain voltages are depicted together with the resulting drain current. The pulses, in particular the drain current, must keep the stable level for a sufficiently long time in order to obtain a reliable measurement. Indeed, due to the very fast rise- and fall-times of these pulses, substantial capacitive charging and discharging is observed, causing the peaks visible at both sides of the pulses. During the planning and initial exploration of the experiment it was decided that 1 μs was the reasonable lower pulse width limit above which reliable measurements in the current ranges of interest could be performed. The actual current measurement window that the instrument uses for determining the output value is indicated in figure 3.18a. At sub-micro-ampere current level the pulse cannot be shortened much further, by doing so the capacitive charging and discharging of the parasitic capacitances would fall into the measurement window hampering a correct estimation of the current level.

Figure 3.19 shows typical I-V sweeps for the full gate bias range. The graph shows the limitations of this type of measurements. For example, through the RPM, the DC measurement is limited by the leakage of the switch that alternatively selects the DC measurement unit and the PMU, in this case about 1 nA. For the shortest pulses, the current meter can be used down to the 100 μA range according to the specifications [81]. This brings the lowest detectable current values up to the order of 100 nA (which is 0.1 % of the full range of the current meter). This is why the current levels off and stays constant for gate

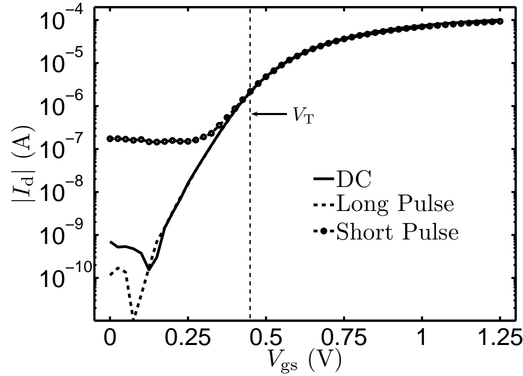


Figure 3.19: Drain currents measured with the PMU with two different pulse widths and a standard DC measurement.

voltage below 0.3 V (black line with solid circles in figure 3.19).

A schematic representation of other relevant pulse variables is depicted in figure 3.20. The pulse used in the experiment has two voltage levels: the so-called base level and the pulse (measure) level. The base level is the voltage applied before and after the actual measure pulse. This level is applied for 100 ms prior to the measure pulse, determining therefore the initial condition of the device before each measurement. The pulse level is kept constant for the time specified by the pulse width variable. The picture sketched in figure 3.20 is merely an explanatory representation; the pulse level can in fact be (and sometimes indeed is) lower than the base level. The pulses applied to the gate and drain terminals have equal timing but different voltage levels. The PMU connected to the drain always uses the same base and pulse levels in the reported experiment, 0 V and 0.05 V respectively. In other words, a non-zero voltage will be applied to the drain only for the same time as the gate pulse. The pulses applied to the gate, on the other hand, were varied both in terms of base level (pre-soak) and the actual pulse (measure) level (the sweeping variable). As indicated before, the base level is used to pre-charge traps. This voltage is kept constant (hence pre-soak) during the initialization time for 100 ms. Three levels of pre-soak were tested: 0 V (depletion), 0.4 V (moderate inversion) and 1 V (strong inversion). During these pre-soaks, oxide traps are supposed to be filled (or emptied) before the actual measure pulse is applied. The gate pulse level is swept from 0 to 1.25 V with 25-mV steps for a full $I_d - V_{gs}$ transfer characteristic. Two pulse widths were tested: 1 μs and 100 μs.

Finally, as further subject of investigation, the impact of hot carrier damage

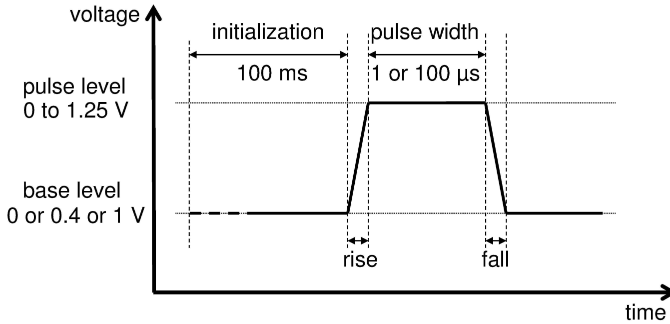


Figure 3.20: Schematic representation of the pulse variables. The pulse settings apply to the gate and drain terminals while source and well are grounded. The rise and fall times are always set to be 2 % of the selected pulse width.

on DC and DC pulsed mismatch standard deviations is evaluated. By applying an HCI stress on a DC characterized population, the density of interface states was increased substantially. The DC measurements were repeated on the HCI stressed devices and subsequently compared to the pulsed measurements. The device were stressed for 100 s applying 2.4 V on the drain and 1.2 V on the gate. This stress resulted in a typical average V_{T} shift of approximately 40 mV, which was sufficient to generate enough traps to affect the mismatch signatures [82].

3.5.2 Results and discussion

The main purpose of the study was to establish whether statistically significant differences could be observed between the mismatch signatures of the devices under test, when standard DC measurements are compared to pulsed measurements. The actual comparison between DC and pulse measurements (PM) with different settings is performed mostly using the fluctuation sweep, i.e. the standard deviations of the relative drain current mismatch. The autocorrelation plot will only be shown for the comparison of the pulse widths.

If the fluctuations of interface states (with a reaction time at least longer than 1 μs) were to play a role in the drain current mismatch in the weak inversion region, differences both in the magnitude and in the shape of the fluctuation sweeps obtained on the same populations but with different measurement conditions should be visible. Apart from the verification of the observed and simulated relation between interface states and mismatch signatures, this experiment was also aimed at possibly bridging the gap between matching and 1/f noise.

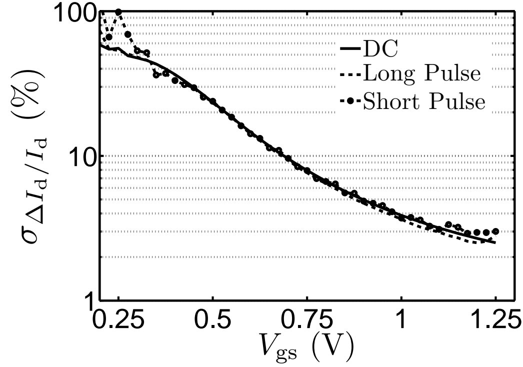


Figure 3.21: Comparison between fluctuation sweeps of standard DC measurements and pulse measurements both with base level of 0 V but different pulse widths (1 μs and 100 μs for short and long pulse respectively).

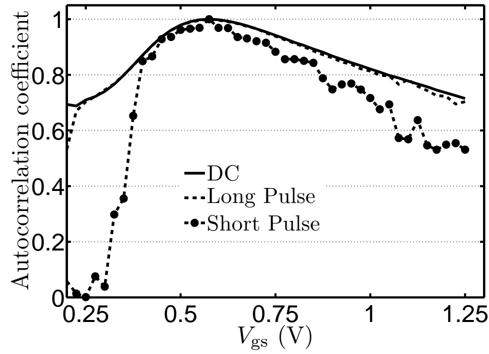


Figure 3.22: Comparison between autocorrelation plots of standard DC measurements and pulse measurements both with base level of 0 V but different pulse widths (1 μs and 100 μs for short and long pulse respectively).

As explained in the previous section, the leakage of the switch (in case of standard DC measurements) and the high current range (limited lower level) limit the gate voltage range on which good results could be obtained (figure 3.19). Given these considerations and for better readability of the graphs, the gate voltage range on the x-axis in figures 3.21 to 3.24 begins at 0.2 V instead of 0 V.

Pulse length comparison

Mismatch fluctuation sweeps for the standard DC (measured on the same devices and shown as reference) and PM with base level 0 V and the two pulse lengths are depicted in figure 3.21. The pulsed measurements worked very well: no “unphysical” behavior, range switching, substantial peaks or unexpected humps are visible. The three curves show no significant differences in the weak and moderate inversion region where the interface states related fluctuations were supposed to have the biggest impact [43]. From these observations one would have to conclude that if interface states affect mismatch, they must be interface states that are not probed by this technique, i.e., interface states faster than 1 μs.

The autocorrelation plot, shown in figure 3.22, leads to the same conclusions. In fact, the DC curve and the ‘Long Pulse’ are on top of each other while for short pulse the de-correlation for high $V_{\rm gs}$ is slightly more pronounced. This is, however, explainable by the fact that the current mismatch measured with the short pulse is quite ragged, due to the limited resolution of the current meter in this range. Such measurement noise automatically reduces the autocorrelation coefficient.

Pre-soak level comparison

The measurement technique works. Now the impact of interface state “preconditioning” is investigated by comparing pulsed-matching measurements obtained using different pre-soak conditions. Note that it is known from switched 1/f noise measurements that low-frequency noise, and thus most likely the underlying slow oxide traps, are affected by the pre-soak charging states of these traps [78, 79]. Figure 3.23 presents fluctuation sweeps of pulsed measurements with the short pulses (1 μs) but using different base levels. The initial condition (pre-soak) has no impact on the level of mismatch or on the shape of the fluctuation sweep. Again, the same conclusions can be drawn from our pulsed matching measurements: either the interface states have charging and discharging time constants substantially below 1 μs or interface state fluctuations do not significantly contribute to the mismatch at all.

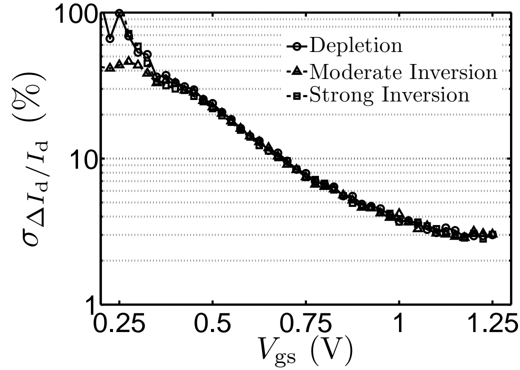


Figure 3.23: Comparison between fluctuation sweeps of pulse measurements all with the shortest pulse but with different base levels (0 V, 0.4 V and 1 V for depletion, moderate inversion and strong inversion respectively).

Stressed devices

It remains now to verify whether, after adding more traps through HCI stress, their effect is visible in pulsed measurements. The fluctuation sweeps of standard DC measurements before and after stress and of PM (both for short and long pulse with 0 V as base level) are depicted in figure 3.24. The stress has substantially impacted the mismatch performance of the devices in strong inversion. Nevertheless, again no difference is observed between DC and PM in weak inversion also for the HCI stressed device populations.

Similarly, for the sake of completeness, the mismatch signature of fresh and stressed device measured with regular DC equipment (the Keithley 4200-SCS) are compared.

The fluctuation sweeps resulting from these measurements are shown in figure 3.25. Beside the shift of the threshold voltage, the magnitude of the resulting mismatch is basically unaffected by the additional traps created by the stress. The new mismatch component that is brought in by the interface states is somehow compensated by the increase in the subthreshold slope due to the deterioration of the interface created by the traps (this is discussed in more detail in chapter 5, see equation 5.1).

The autocorrelation plot obtained with measurements on stressed devices does have a different shape and magnitude in subthreshold (see figure 3.26). As a matter of fact, the correlation of the mismatch in subthreshold with the mismatch at threshold voltage decreases substantially and does not level off as

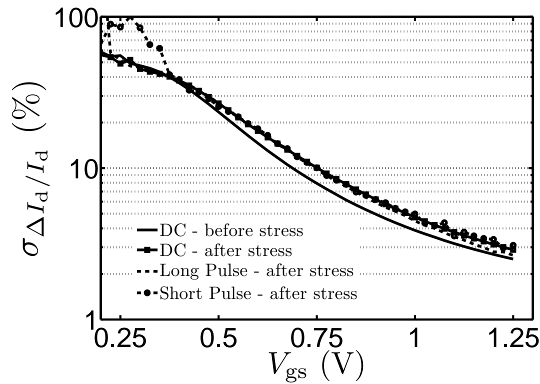


Figure 3.24: Comparison between fluctuation sweeps of DC and pulse measurements performed on stressed devices. The DC fluctuation sweep on fresh device is shown here as reference.

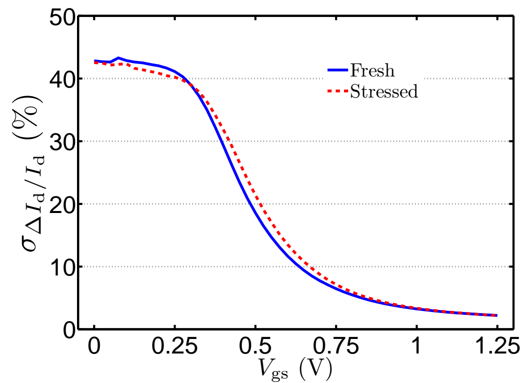


Figure 3.25: Comparison between fluctuation sweeps obtained on fresh and HCI stressed device (DC measurements).

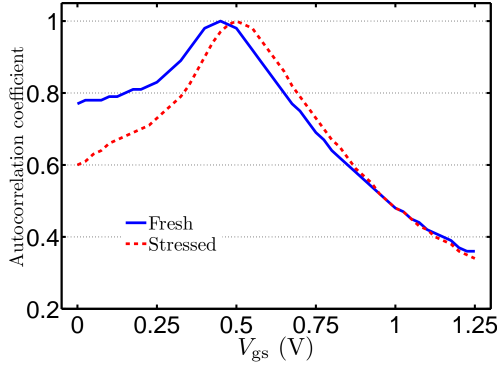


Figure 3.26: Comparison between autocorrelation plot obtained on fresh and HCI stressed device (DC measurements).

it happens in case of fresh devices. This phenomenon is due to an increase of the subthreshold slope variations in the stressed devices compared to fresh ones, the threshold voltage mismatch remains in fact basically unaltered [82]. It must be noted that the shape of the autocorrelation plot after stress is remarkably similar to the simulation with RIF first version (see figure 3.7). This could be seen as a confirmation of the discussion of section 3.4. The HCI stress is usually localized resulting in a more 'blocking nature' of the charges.

3.6 Conclusion

Through a new analysis method, based on mismatch signatures, PCA and statistical device simulations, a presumed impact of interface states on MOS transistor mismatch in moderate and weak inversion is explored.

It is found that different implementations of interface states fluctuations in the SiSPET statistical device simulator lead to quite different results. It is undeniable that something happens with the drain current mismatch standard deviation in subthreshold that is not strongly related to RDF. Of all the root cause proposed in literature, interface state fluctuations still remain the most plausible one. However, from the contrasting outcomes of the different simulations, one might argue that simulation alone is not the best approach to answer the question which phenomenon is responsible for the de-correlation below threshold. A better result might be obtained when the interface trap population is properly characterized (using charge pumping, C-V and perhaps

other techniques) on the same wafer that is studied for its matching behavior, this is however not trivial for the low trap density in combination with small devices. The simulations could then be carried out with the same experimentally established total density and probability density functions for the interface states.

Furthermore, a successful microsecond pulsed DC MOSFET matching measurement down to nano-amperes current levels is reported. This was done to study MOSFET mismatch in weak inversion under pulsed DC conditions. The experiment suggests that if any interface states seriously affect the mismatch in weak and moderate inversion, they are faster than 1 μs (which is not unlikely according to the literature). Instrumentation limitations make probing this low-current regime at shorter time scales impossible at the present state of the art. Also when the density of interface states is substantially increased through HC stress, the expected different mismatch signatures with pulsed I-V in moderate and weak inversion are not observed while the literature does report enhanced 1/f noise levels.

A possible implementation of the de-correlation of the relative drain current mismatch between weak and strong inversion regions in contemporary MOS transistors in a compact model has been proposed. This implementation might also be applicable when the cause of the de-correlation is different from interface state fluctuations as long as the effect can be described as independent (from threshold voltage variation) subthreshold slope fluctuations which is also reported.

As future work, it is recommended a thorough study on 3-D effect of interface states (or work-function fluctuations in case of metal gate) in order to resolve this issue that can become really important in case of high-K / metal stacks [83] or other somewhat more exotic compounds, e.g., GaN, or C, that usually suffer from high concentration of traps and defects. Advances in measurement techniques for a better characterization of interface states could be also a possible way to improve the understanding on this field. Future research in characterization could focus on improving present pulsed or high-frequency measurement techniques in order to help in identifying the root cause of the de-correlation or other mismatch effects.

Chapter 4

Mismatch in LDMOS Devices

In the previous chapter our modified TCAD simulations and our analysis methodology were applied extensively to study contemporary bulk MOSFETs. In this chapter the same tool and techniques are used to study of the influence of different sources of DC parametric mismatch in a device with a different architecture. The device under test is a Lateral Diffused MOS (LDMOS) transistor.

The chapter is structured as follows: in the first section a brief introduction and motivation is given. The second section describes the device under test, then in the third section the measurement results are illustrated and analyzed. The simulation results are presented in the fourth section after which the chapter is concluded.

4.1 Introduction

The LDMOS transistor architecture is widely used in RF applications, base stations, radar and broadcast applications because of its high voltages capabilities combined with good RF performance [84, 85]. In monolithic microwave integrated circuits, this device is also used in analog circuit block implementations under relatively "low power" conditions. The standard DC parametric mismatch performance becomes important for the functionality of such blocks, an example of medical application is reported in [86]. A first attempt to address this topic has been done by Posch *et al.* [87, 88]. They focus on the matching performance in the high-voltage regime and on the measurement challenges as-

sociated to the characterization of these devices. Differently, in this chapter, by comparing measurements and statistical simulations, the impact on mismatch of the most important fluctuation causes is qualitatively evaluated through parameter extraction and mismatch signature of LDMOS transistors when used in DC and low-voltage regime.

The study was requested to investigated a yield problem of LDMOSs employed in current mirrors in actual production chips. The aim of the experiment was to investigate whether the yield loss came from an intrinsic problem of the device itself or from an overlooked technology flaw. In particular, the effect of the shape of the doping profile in the channel, the interface states and the series resistances on the mismatch in different operating regions of the device formed the main focus points of this investigation.

4.2 Device description

The device investigated in this work is representative of a class of RF-LDMOS transistors fabricated by NXP Semiconductors [84]. A simplified version of the actual LDMOS is created with Synopsys' Structure Editor [37] and simulated with the 2-D Sentaurus Device simulator [36]. A schematic cross section of such a structure is shown in figure 4.1. The channel region is defined by the lateral diffusion of a p-type implantation from the source side of the transistor. This means that the doping in the channel area has a strong non-uniformity along the lateral direction. It is typically about 0.3-μm long. A lightly n-type doped region (drift region) defines the end of the channel area and extends for about 3 μm in these simulations. The channel and the drift region are overlaid with silicon oxide (several tens of nm thick). In this type of device, the gate electrode covers only the actual channel area leaving the drift region largely gate-bias independent as is generally the case in LDMOS transistors for RF applications. The dimensions, the doping values and some mobility model parameters have been adjusted (calibrated) in such a way to obtain performances as close as possible to measurements, as it was done for MOSFETs and explained in section 2.3.

4.3 Measurements

4.3.1 Experimental methodology

The characterization of the LDMOS has been carried out with a Keithley 4200 Semiconductor Characterization System and a Cascade 12k semi-automatic

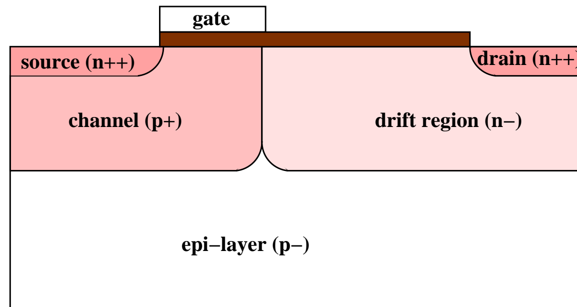
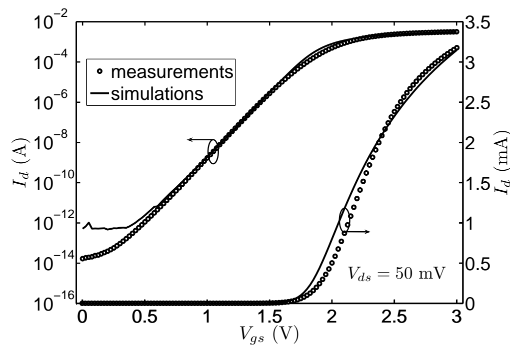
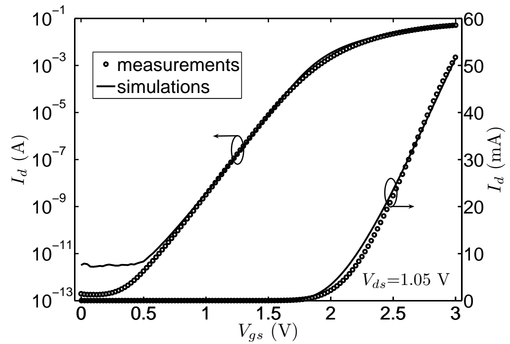


Figure 4.1: Schematic cross section of the simulated LDMOS transistor.



(a)



(b)

Figure 4.2: Calibration results. Median drain currents of measurements (symbols) and simulations (lines) in linear and logarithmic scale for both drain-source biases, 50 mV (a) and 1.05 V (b).

wafer prober. Unlike the test structures presented inchapter 2 (section 2.4), these devices, being actual products, are not placed in a matched pair kind of layout with common source and common body. Thus, parametric mismatch is evaluated by sequentially measuring two identically designed transistors (width of approximately 1300 μm) at minimum allowed distance, i.e. about 1100 μm between the two transistors of the pair. These so-created "pairs" are spread out evenly over a 200-mm wafer and measured 84 positions. In order to increase the statistical confidence of the experiment the measurements are repeated on a fresh population (identical pairs on a different reticle position on the die). In principle there should be no difference between these two populations. For sake of simplicity they are referred to as 'A' and 'B'. Although devices that form a pair are not at the small distance normally applied for matched pairs (< 100 μm), the contribution of the deterministic gradient across the wafer can be considered negligible compared to the random fluctuations. This will be substantiated in the next section.

The drain current of the LDMOS under test is measured at two different drain biases ($V_{\text{ds}} = 50$ mV and 1.05 V) while sweeping the gate voltage, $V_{\text{gs}} = 0$ to 3.0 V with 25-mV steps. The current of a typical device is plotted and compared with the results of TCAD simulations in figure 4.2. The simulated LDMOS reproduces the measurements very well, with the exception of low gate biases where the measurements and the simulations are dominated by junction leakage which is not tuned for this study.

4.3.2 Results

Measurements of the full gate voltage sweeps are employed to evaluate the mismatch signature, as explained in section 2.4.2, and to extract (from measurements with $V_{\text{ds}} = 50$ mV) the threshold voltage, V_{T}, and the current factor, β, employing three-point extraction with fixed gate overdrive (see section 2.4.1).

The mismatch signatures of the two measured populations are depicted in figure 4.3. The drain current mismatch goes to very high values below 0.7 V due to junction leakage (which varies quite substantially) as seen in figure 4.2. For a good readability of the graphs the range of gate voltages plotted for the two figures thus starts at 0.7 V. A detailed investigation of the leakage mechanisms is outside the scope of this study because that voltage range ($V_{\text{gs}} < 0.7$ V) will hardly be used as operational regime.

The signatures in weak and moderate inversion of both populations is similar to the one generally observed for conventional CMOS transistors. However, the signature of population 'B' indicates that an additional fluctuating component dominates the mismatch fluctuations in strong inversion ($V_{\text{gs}} > 2.2$ V).

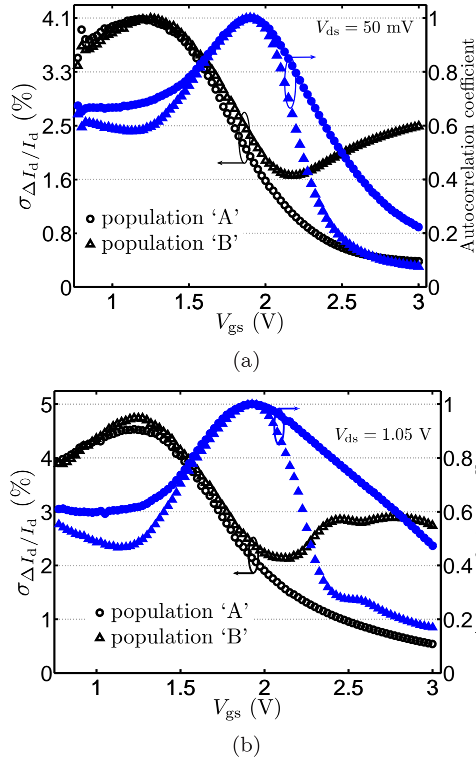


Figure 4.3: Mismatch signature of the two measured populations, $V_{ds} = 50$ mV (a) and $V_{ds} = 1.05$ V (b).

Also, the strong de-correlation between the mismatch at threshold voltage and at biases above threshold is more pronounced for population 'B'. This large fluctuation is ascribed to a series resistance variation attributed to a non-ideal probe-to-pad contact. This assumption is verified with simulations later in the chapter (see section 4.4.3).

In an attempt to avoid that these resistance fluctuations hamper the extraction of V_T and β, the gate overdrives ($V_{gs} - V_T$) were limited up to 0.7 V ($V_{gs} < 2.5$ V). This led to approximately the same standard deviations of V_T and β mismatch for both populations. The standard deviation of the threshold voltage mismatch of $\sigma_{\Delta V_T} = 2.0$ mV and the standard deviation of the relative current factor mismatch of $\sigma_{\Delta\beta/\beta} = 1.2$ %, correspond to area factors of $A_{\Delta V_T} \approx 35$ mVμm and $A_{\Delta\beta/\beta} \approx 21$ %μm when the σ's are scaled with the

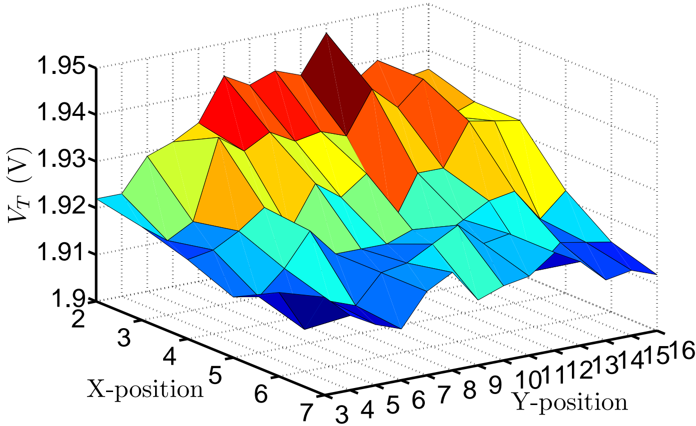


Figure 4.4: Threshold voltage gradient across the wafer. A clear tilt is visible in this wafermap.

estimated channel area following Pelgrom's law [2]. This area factor of beta mismatch is extremely large when compared to what is expected in standard CMOS technologies (less than 2 %μm [63]). Also, the relative drain current mismatch for population 'A' goes down to about 0.5 % for $V_{\mathrm{gs}} > 2.5$ V (in figure 4.3), while, in principle, the drain current mismatch in the strong inversion regime should be very close to the standard deviation of $\Delta\beta/\beta$ fluctuations [2].

For these devices a combination of three-point extraction (for threshold voltage evaluation) and mismatch signatures (for drain current mismatch evaluation) has been used. This combined method is therefore also used to study how intrinsic device characteristic variations such as different channel doping profiles, dopants and interface states fluctuations as well as external factors, e.g., probe-pad contact resistance fluctuations, affect LDMOS transistor mismatch.

Before analyzing the causes of mismatch in detail to identify which one is the main cause of a larger-than-expected mismatch it should be demonstrated that the contribution of the gradient across the wafer is negligible. While for β no clear gradient pattern across the wafer is visible, meaning that the random variation is much larger than the gradient, for the threshold voltage a clear gradient is present. In figure 4.4, a wafer map of the measured threshold voltage is shown. A significant gradient is visible as a tilted plane. It should be noticed however, that at the maximum distance of approximately 200 mm the

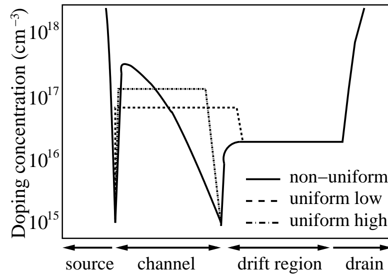


Figure 4.5: Representation of the three doping profiles used in RDF-only simulations.

difference in threshold voltage is only 26 mV and it can be assumed linear to first order. Given the 1-mm distance between transistors in a pair the gradient is 0.13 mV, which is more than an order of magnitude lower than the measured standard deviation and therefore it can and will be neglected.

4.4 Simulations

The study of the possible impact of well controlled perturbations to the LD-MOS device DC parametric mismatch is performed using the device simulation capabilities of SiSPET. Three different mismatch contributors are applied to a tuned device through the doping and interface states randomizer (see [43] and section 2.2.2) and then simulated using Sentaurus Device. The area, over which the doping and the interface states randomizations are applied, covers the channel as well as the drift region. For a good trade-off between computing time and statistical uncertainty the population size is chosen at 51.

4.4.1 Influence of channel doping profile

One of the original hypotheses was that the observed mismatch enhancements as presented in the paragraph 4.3.2 could arise from the strong lateral non-uniformity of the channel doping. This has been reported, for instance, in long MOSFETs with pocket implantations [31, 89, 90]. To investigate this, random doping fluctuation perturbations have been applied, not only on a representation of a realistic laterally-diffused channel doping profile but also on two other devices with artificial constant doping levels. A schematic representation of the three lateral doping profiles is sketched in figure 4.5. The two constant doping profiles have different levels and channel lengths. The doping levels and

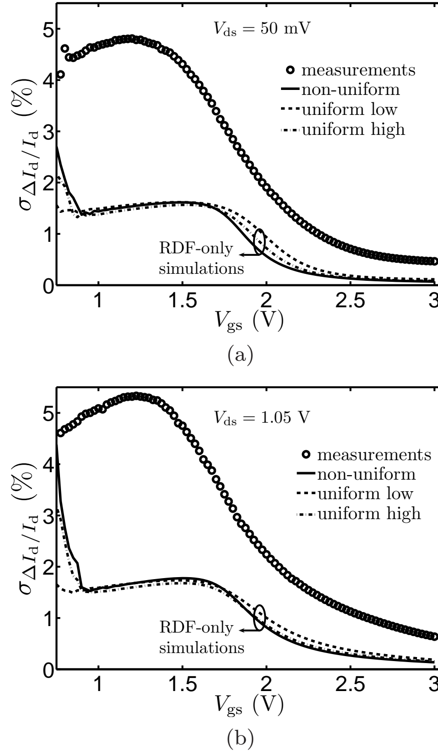


Figure 4.6: Comparison between the fluctuation sweeps of measured devices (population 'A') and RDF-only simulations with three different doping profiles, V_{ds} = 50 mV (a) and V_{ds} = 1.05 V (b).

the channel lengths have been chosen to reproduce approximately the same threshold voltage and current delivered as the measured ones.

The fluctuation sweeps of the three configurations, simulated with RDF-only, are compared with the measurements of population 'A' in figure 4.6. For a fair comparison, the drain current mismatch from the device with a longer channel has been divided by an effective length through $\sqrt{L}$. All three simulated curves show similar behavior but they all deviate strongly from the measured levels. Thus, when only RDF is taken into account, shape and level of the channel doping apparently have little influence on the overall mismatch performance considering both drain-source biases. Furthermore, the standard deviations of the threshold voltage mismatch and the relative beta mismatch extracted for the three configurations are approximately the same and much lower than the measured values. Being a uniform doped device, the theoretical standard deviation (and thus the area factor) of the threshold voltage mismatch caused by RDF can be obtained with the Stolk-Widdershoven equation [6]:

$$\sigma_{\Delta V_{\mathrm{T}}} \approx \left(\frac{\sqrt[4]{4q^3 \epsilon_{\mathrm{Si}} \varphi_{\mathrm{B}}}}{\sqrt{3}} \right) \cdot \left[\frac{k_{\mathrm{B}} T}{q} \cdot \frac{1}{\sqrt{4q \epsilon_{\mathrm{Si}} \phi_{\mathrm{B}} N_{\mathrm{A}}}} + \frac{T_{\mathrm{ox}}}{\epsilon_{\mathrm{ox}}} \right] \cdot \frac{\sqrt[4]{N_{\mathrm{A}}}}{\sqrt{WL}} \tag{4.1}$$

where q is a single electron charge, ϵ_{Si} and ϵ_{ox} are the permittivity of silicon and oxide respectively, T is the absolute temperature, k_{B} is the Boltmann constant, T_{ox} is the oxide thickness, $\varphi_{\mathrm{B}} = 2k_{\mathrm{B}}T/q \cdot ln(N_{\mathrm{A}}/n_i)$ with n_i the intrinsic carrier concentration and N_{A} the doping concentration. For the 'uniform low' device the simulated standard deviations of the threshold voltage mismatch and relative current factor mismatch are $\sigma_{\Delta V_{\mathrm{T}}} = 1.1$ mV and $\sigma_{\Delta\beta/\beta} = 0.1$ %. So, calculating the area factors, we obtain: $A_{\Delta V_T} \approx 20$ mVμm (while $A_{\Delta V_{\mathrm{Ttheory}}} \approx 19$ mVμm using equation 4.1) and $A_{\Delta\beta/\beta} \approx 1.8$ %μm. Given these observations, RDF alone cannot explain the large observed mismatch and additional sources of fluctuation must be significant in the studied devices.

4.4.2 Other sources of mismatch

As shown already earlier in this thesis, the strength of random-fluctuation simulations lies in the possibility of combining and precisely controlling alternative fluctuation causes practically unachievable by technological experiments and measurements. For the LDMOS two sources of fluctuations were added on top of RDF: random interface states and random series resistance fluctuations. It is worth pointing out that the aim of these simulations is to obtain a qualitative description of the impact of a certain fluctuating source on the mismatch behavior, rather than to give a quantitative analysis. This study is focused at

identifying mechanisms that can be held responsible for the observed matching degeneration. Thus, it should not be interpreted as a method for extracting interface state densities or series resistance fluctuations.

As explained in [43] and chapter 3, interface states can have a big impact on the mismatch performance of a MOS transistor as long as random energy, concentration and position are considered. Thus, also for LDMOS random interface states are assigned to the interface between the gate oxide and the silicon but in this case the energy is randomly selected in the bandgap of the silicon and the nominal concentration follows a parabolic shape that ranges from $1{\cdot}10\ \text{cm}^{-2}$ at midgap to $5{\cdot}10\ \text{cm}^{-2}$ at the borders of valence and conduction bands. RIF should primarily affect the mismatch below threshold.

Above threshold, however, the increase of the fluctuations is affected by series resistance fluctuations [54]. The currents delivered by these 1300-μm wide test devices are of the order of milliamperes even at low drain bias (figure 4.2). This means that a significant potential can drop over a contact resistance of few tenths of an Ohm. To investigate this impact on the mismatch signature, two series resistances are assigned to the source and drain electrodes and randomly varied. In order to reach the two levels of fluctuation in strong inversion (for the two measured populations), as shown in figure 4.3, two different ranges of resistances, representing a ‘bad’ and a ‘good’ probe-pad contact, are simulated. The variations, around a median value of 1 Ω, are chosen from a uniform (square shaped) probability density function at ± 0.3 Ω and ± 0.05 Ω for the ‘bad’ and the ‘good’ contact respectively (for the actual implementation see section 2.2.3).

4.4.3 Discussion

Figure 4.7 shows the fluctuation sweeps of simulations when RIF and RSR are individually added to the original population with RDF with the non-uniform doping. On the same figure the fluctuation sweep resulting from the simulation with RDF-only from measurements of population ‘B’ is plotted for comparison. As expected, RIF primarily affects the mismatch in subthreshold and weak inversion regions while the effect of RSR is only visible in strong inversion. The level of mismatch in weak and moderate inversion is much better described by the combination of RIF and RDF (the current is too low in this region for the RSR to contribute) whereas the mismatch in strong inversion measured on population ‘B’ is very well matched by the inclusion of RSR (using the ‘bad’ contact fluctuations). Also, the standard deviations of V_T and β mismatch now reach values comparable to the measurements: 2.3 mV and 0.8 % for $\sigma_{\Delta V_\text{T}}$ and $\sigma_{\Delta\beta/\beta}$, respectively. It is worth noticing that, unlike what was found for

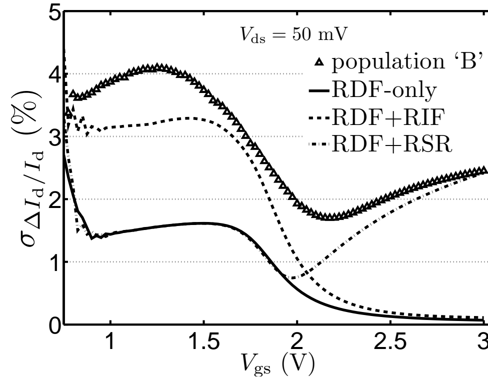


Figure 4.7: Fluctuation sweeps for simulations (lines) of different sources of mismatch added singularly to RDF and measurements (symbols).

standard CMOS technologies, RIF strongly affects beta mismatch in LDMOS device populations when characterized near the peak transconductance point.

When including both extra-sources simultaneously and using two levels of RSR the overall result is very good (see figures 4.8 and 4.9). In the strong inversion region, the simulations with the two properly tuned levels of RSR match very well with the two measured populations and in weak and moderate inversion no clear difference can be seen using different RSR. The autocorrelation plot confirms the need of these additional independent fluctuation sources for a good description of the overall mismatch behavior. However, some discrepancies still remain in the moderate inversion region of the fluctuation sweeps (between 1.8 V and 2.5 V in figure 4.8(a)), and between the autocorrelation plot of the simulated 'good' contact and the population 'A' ($V_{gs} > 2$ V in figure 4.8(b)). These differences could most likely be minimized by optimizing the interface state density and energy distributions. As discussed in section 3.4, the exact position of the channel-blocking most active interface states right at the point where the doping is highest could amplify the fluctuation effect for these 2-D simulations. Further detailed analysis of this effect would be a good starting point for future work. Note that the analysis performed on the curves at $V_{ds} = 1.05$ V (figure 4.9) yields even better agreement.

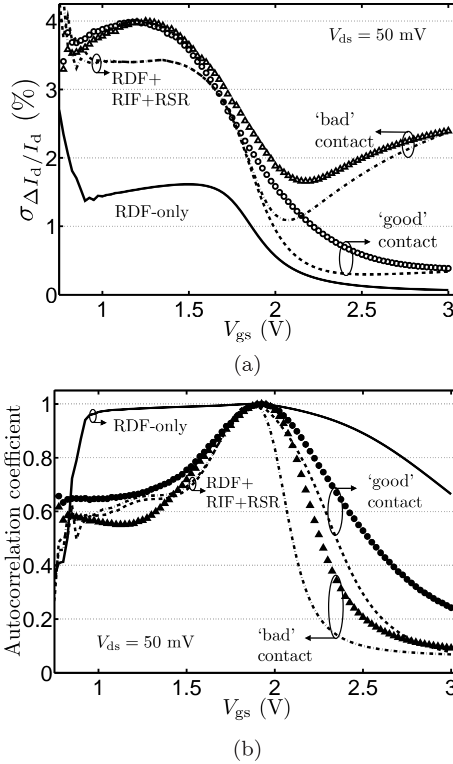


Figure 4.8: Fluctuation sweeps (a) and autocorrelation plot (b) for simulations of different sources of mismatch (lines) and measurements (symbols) with $V_{ds} = 50$ mV.

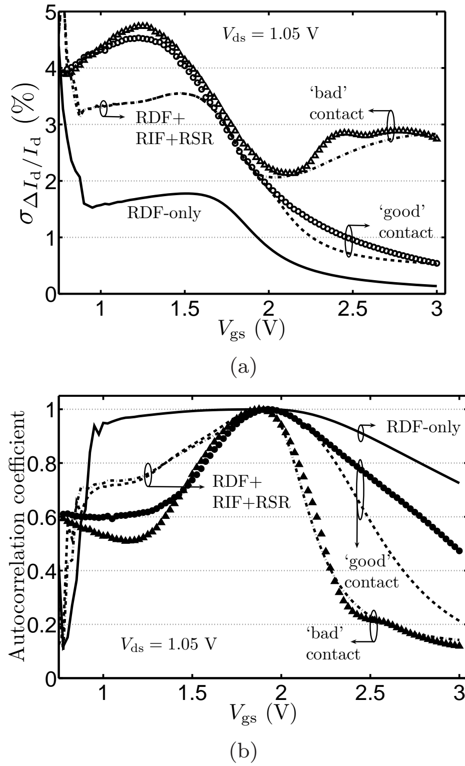


Figure 4.9: Fluctuation sweeps (a) and autocorrelation plot (b) for simulations of different sources of mismatch (lines) and measurements (symbols) with $V_{\text{ds}} = 1.05$ V.

4.5 Conclusion

This chapter applies the mismatch signature techniques and statistical simulations to investigate parametric mismatch fluctuation causes in industrial LDMOS devices. Measurements on transistor pairs show relatively large drain current mismatch fluctuations in all regions of operation. Three sources of fluctuations have been analyzed and compared to measurements. It was found that, if only random dopant fluctuations are taken into account, the shape and level of the channel doping cannot explain the observed mismatch behavior of this category of MOS devices. On the other hand, random interface states significantly affect the behavior of the device in subthreshold as well as in moderate inversion, also increasing the fluctuations of the extracted current factor beta. Finally, particular care must be taken during the characterization of these devices in terms of probe-pad contact resistance, as series resistance variation can easily dominate the extracted fluctuations at high gate biases as well as transistor current mismatch in case of asymmetrical layouts.

Chapter 5

Temperature dependence of mismatch

ICs are typically supposed to work in a range of temperature that goes from -40 °C to +85 °C. The whole functionality of the chip needs to be ensured at all temperature in that range, this includes mismatch performances. It is therefore of great interest to quantify, if present, the impact of temperature on MOS transistor mismatch. In this chapter a study on MOSFET mismatch as a function of temperature for different dimensions, types and technology nodes is presented.

This chapter is structured as follows: first the motivation for this study is given and the measurement methodology is described. Then an overall impression of the impact of temperature on mismatch is given through fluctuation sweeps. The subthreshold region is studied in detail in the following section with the help of a simple model. Then, the strong inversion part is analyzed by comparing the change with temperature of some main mismatch parameters and also by quantifying the drift of drain current mismatch in **individual** pairs. Finally, some conclusions and recommendations for future work are given in the last section.

5.1 Introduction

Any circuit and chip in commercially available products must be fully functional over a specified temperature range, typically -40 °C to 85 °C. This does

not mean that the chip must simply "survive" extreme temperatures. Its performance should be within the specifications at any temperature in the specifications range. Therefore, besides well-known consequences of temperature changes such as mechanical strain due to material expansion and nominal performance changes, the mismatch behavior should be considered as well. In particular, some high-precision circuits such as, bandgap and frequency references or operational amplifiers, will suffer from a possible mismatch drift even after trimming techniques [91, 92, 93].

Despite the fact that this concern is widely spread among circuit designers the subject has been scarcely discussed in open literature in the past. The first to postulate negligible temperature dependence in 3-μm CMOS current mismatch was Lakshmikumar *et al.* [21] in 1986. Then, a first characterization of an improvement with higher temperature of threshold voltage and drain current mismatch was done by Tan *et al.* for 0.18-μm CMOS almost two decades later [94]. More recently, a few characterization studies on modern technology nodes (e.g., 65 nm and 45 nm) have been presented showing again reduction of the mismatch of some parameters at higher temperature [95, 96, 97]. Finally, also some simulation studies were presented on the thermal energy influence on weak inversion current variation in bulk CMOS [98] and temperature-dependent mismatch even in 16-nm SOI FinFETs [32].

A MOSFET's drain current is significantly affected by the temperature and the underlying physics is well understood. In figure 5.1 the median currents of a population of short channel transistors fabricated in a 45 nm technology is shown versus gate voltage. The impact of temperature on drain current is well known, e.g. [99]: the drain current reduces in strong inversion due to a reduction of the mobility while in weak inversion and subthreshold it increases due to higher subthreshold slope.

In this chapter, the temperature effects on mismatch properties for four different technology nodes, namely C14, C90, C65 and C45, are discussed. These CMOS technology nodes are currently in use for analog circuit production. The numbers represent the allegedly channel length of the shortest transistor in nanometer, for C14 the number actually comes from 0.14 μm, so 140 nm. Measurements have been performed for six temperatures in a temperature range of 0 °C to 125 °C under several operating conditions. The devices analyzed per technology always consisted of populations of a statistically relevant number of devices with nominal (i.e. shortest allowed) gate length (different for the four process nodes) and 1 μm (common to all), both with a 1-μm channel width. Both PMOSTs and NMOSTs are considered in the experiments. In this way, the general temperature effects on mismatch is studied as well as the trend and differences across different MOSFET generations. The population

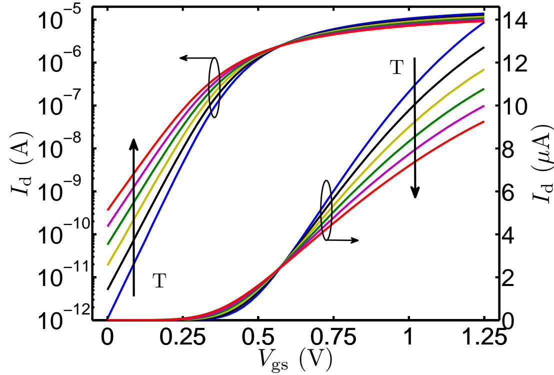


Figure 5.1: Median values of drain current at different temperatures in logarithmic and linear scale for the shortest devices in C45 (V_{ds} = 50 mV). The temperature increase reduces the current in strong inversion (lower mobility) and increases the subthreshold current (lower V_T and higher leakage).

Table 5.1: General information about the technologies under test.

Technology nodes	Shortest gate length (nm)	Population size	V_{gsMAX} (V)	V_{dsMAX} (V)
C14	160	91	1.8	1.8
C90	100	77	1.25	1.2
C65	60	119	1.25	1.2
C45	40	119	1.25	1.1

sizes, the shortest drawn gate length and the used maximum voltages are listed per technology in table 5.1.

The technology nodes considered for this experiment cover a time span of 8 to 10 years of CMOS technologies. The oldest one (C14) is still widely used for many high-performance mixed-signal products. It is difficult to outline all the precise differences in architecture between these processes (for some of them no precise process information is available, as explained in section 2.3) but from the ITRS roadmap [56] the main developments that distinguish one CMOS generation from another can be extracted.

Although the processes do not all come from the same foundry, the underlying architecture is the same for all: bulk MOS with silicon-dioxide based

gate dielectric (oxynitride for C65 and C45) and polysilicon as gate electrode. Already in C14, and thus also for the successive generations, halos i.e., highly tilted implants used to suppress undesirable short channel effect, were introduced. The implanted dose tends to increase with the shrink of the device, more or less according to standard device scaling rules and practices. Another development that is worth to mention is the use of strain in the source and drain regions in C45. Since our test structures are very simple and make a limited use of the back-end part, possible differences that exist among metal stacks of these processes are neglected.

5.1.1 Measurement methodology

The matched pair test structures used for this experiment are described earlier in section 2.4. The devices were measured on 77 to 119 different positions (see table 5.1) spread out evenly over 200- and 300-mm wafers, using a Keithley 4200 SCS and an S300 Cascade prober equipped with an ESR thermo chuck. Before every measurement the chuck is warmed up (or cooled down) until it reaches the desired temperature. The temperature on the thermo chuck is kept constant for a relatively long period before the measurements are started in order to have a temperature as stable as possible. The thermo chuck ensures an accuracy of the temperature of the plate of the order of tenths of degrees. This accuracy is more than sufficient for our purposes. Furthermore, any non-homogeneity in the temperature distribution across the wafer will be mitigated by the fact that transistors of the matched pair are closely spaced. They can be therefore considered at the same temperature.

Drain currents of the two MOSFETs in the pair are measured simultaneously by sweeping the gate voltage, $V_{\mathrm{gs}} = 0 \cdots V_{\mathrm{gsMAX}}$ with a step of 25 mV, at two different drain biases ($V_{\mathrm{ds}} = 50$ mV and V_{dsMAX}) in a range of six temperatures, $T = 0, 25 \cdots 125$ °C. A first analysis has been performed with the help of *fluctuation sweeps* i.e., the standard deviation of the relative current mismatch calculated on the whole population for a full gate bias sweep as described in 2.4.2.

A more quantitative analysis of the changes of mismatch is done looking at the variation of the mismatch of three parameters: the threshold voltage, V_{T}, the current factor, β, and the maximum drive current, I_{ON}. As explained in section 2.4.1 and [30], ΔV_{T} and $\Delta\beta/\beta$ are extracted from the curves obtained with $V_{\mathrm{ds}} = 50$ mV employing the three-point extraction with fixed gate overdrive. This technique includes small fluctuations of parasitic series resistances (as well as probe-pad contact resistances) in the mobility reduction parameter, θ, therefore mitigating its influence on β. ΔI_{ON} is calculated from the satura-

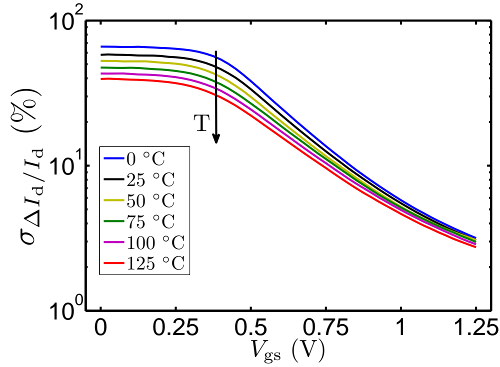


Figure 5.2: Fluctuation sweeps of a population of shortest transistors in C45 ($V_{ds} =$ 50 mV). This trend is representative for all lengths, types and generations considered in this study.

tion current (with $V_{gs} = V_{gsMAX}$ and $V_{ds} = V_{dsMAX}$). These three parameters together are used for obtaining a clear understanding of the variation involved with temperature as they represent the basic of most mismatch models and in general are used as references for comparison of mismatch properties of different technologies. Note however that $V_{gs} - V_T$ (the gate overdrive) is not equal for the different technologies, hence I_{ON} does not necessarily have the same physical interpretation for the four technology nodes.

5.2 Fluctuation sweeps

Representative examples of the temperature effects on MOSFET drain current mismatch are shown in figures 5.2 and 5.3. In these figures the fluctuation sweeps of the same population as in figure 5.1 are depicted at six temperatures for currents measured at $V_{ds} = 50$ mV and 1.1 V respectively. The logarithmic scale has been chosen for the fluctuation sweeps to display the effect of the temperature on the relative drain current mismatch better in strong inversion where the change of the $\sigma_{\Delta I_d/I_d}$ is relatively small. The trend of the fluctuation sweeps shown here for the C45 short transistors is representative for all the types, lengths and generations considered in this chapter.

The first impression of the impact of temperature is indeed that the mismatch of the drain current (considering the whole population) reduces at higher temperature.

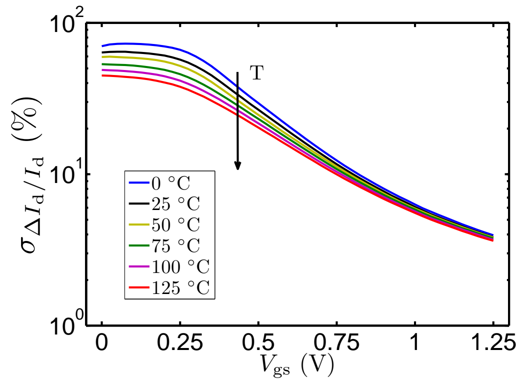


Figure 5.3: Fluctuation sweeps of a population of shortest transistors in C45 ($V_{\mathrm{ds}} = 1.1$ V). This trend is representative for all lengths, types and generations considered in this study.

Particularly evident is the change of mismatch in subthreshold: at the highest temperature the mismatch standard deviation is half of the value measured at the lowest temperature. This phenomenon will be discussed in more details in the next section.

Another observation that can be made from figures 5.2 and 5.3 is that in strong inversion the standard deviation of the relative drain current mismatch also reduces, albeit of a significantly smaller order. Although this trend is quantitatively slightly less pronounced, it is clearer when high voltage is applied on the drain where probe-to-pad contact resistance are less significant.

5.3 Subthreshold mismatch

The subthreshold region is gaining attention and importance due to the demands for power reduction. In fact, circuit designers keep pushing the bias of their devices towards the threshold voltage (and frequently even below) [100]. As it has been outlined before from the fluctuation sweeps (figures 5.2 and 5.3), it appears that relative current mismatch for gate bias below V_{T} significantly decreases when the temperature increases.

The main feature of this behavior is an inverse linear fluctuation reduction with temperature resulting in a relative drain current mismatch decrease of approximately 50 % over the assessed temperature range. This substantial reduction can be understood by considering the standard deviation of the rela-

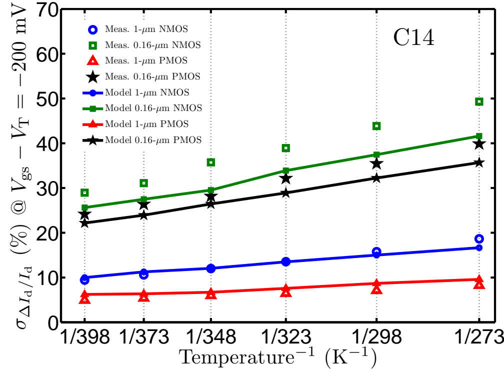


Figure 5.4: Subthreshold mismatch for all the dimensions and types in C14. The measurements are represented in symbols and the model in lines. Circles are 1-μm NMOS, squares are short NMOS, triangles are 1-μm PMOS and stars are short PMOS.

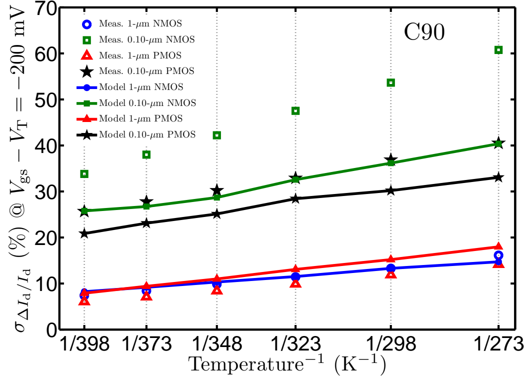


Figure 5.5: Subthreshold mismatch for all the dimensions and types in C90. The measurements are represented in symbols and the model in lines. Circles are 1-μm NMOS, squares are short NMOS, triangles are 1-μm PMOS and stars are short PMOS.

tive drain current mismatch in that region derived from the equation of a MOS current in subthreshold as in [101]:

$$\sigma_{\Delta I_\mathrm{d}/I_\mathrm{d}} \simeq \frac{q\sigma_{\Delta V_\mathrm{T}}}{\eta k_\mathrm{b} T} \tag{5.1}$$

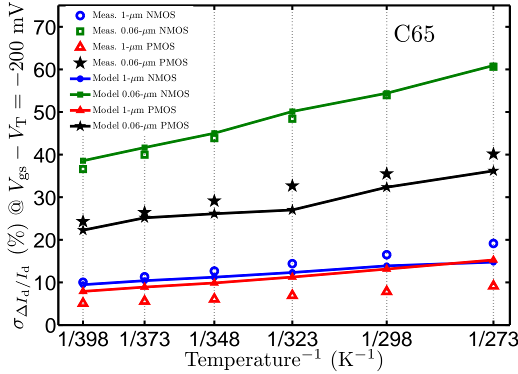


Figure 5.6: Subthreshold mismatch for all the dimensions and types in C65. The measurements are represented in symbols and the model in lines. Circles are 1-μm NMOS, squares are short NMOS, triangles are 1-μm PMOS and stars are short PMOS.

where q is the electron charge, $\sigma_{\Delta V_T}$ the standard deviation of threshold voltage mismatch, η is the ratio between the actual subthreshold slope and the ideal one (∼60 mV/decade at room temperature), k_b the Boltzmann constant and T the absolute temperature. Assuming the threshold voltage mismatch variation negligible with temperature, as it will be shown in the next section, and η only slightly dependent [99], (5.1) is inversely proportional to temperature.

A comparison between measurements and the results of this equation, for all the populations, is shown in figures 5.4 to 5.7. The measured $\sigma_{\Delta I_d/I_d}$ values were obtained for a constant overdrive, $V_{gs} - V_T = -200$ mV and a $V_{ds} = 50$ mV.

The global trend is well captured by the simple model especially for the longer transistors. For the minimum gate length transistors, however, the model slightly underestimates the magnitude of the relative drain current mismatch (even at room temperature) and in two cases also the slope seems to be off (C14 and C90 short NMOS). Note that the value of $\sigma_{\Delta V_T}$ used in the model equation is the one extracted from the measurements at each temperature. The discrepancies between the model and the measurements can be explained by the fact that the V_T extraction is not necessarily related to the mismatch in subthreshold where other effects uncorrelated to V_T can be important (e.g. interface state fluctuations). Equation (5.1) as proposed here is not meant to give a thorough description of the phenomena involved or to substitute more accurate, though more complicated, models, e.g., BSIM and PSP. Yet even this

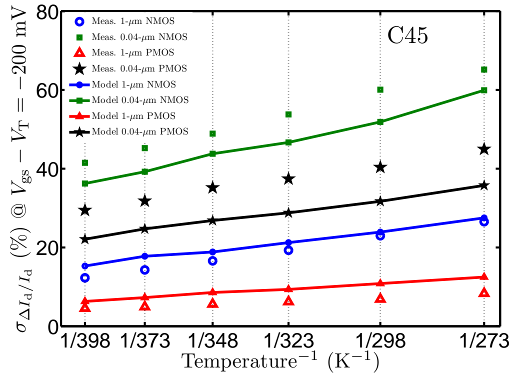


Figure 5.7: Subthreshold mismatch for all the dimensions and types in C45. The measurements are represented in symbols and the model in lines. Circles are 1-μm NMOS, squares are short NMOS, triangles are 1-μm PMOS and stars are short PMOS.

simple formula can capture quite well the qualitative impact of temperature on MOSFET mismatch in subthreshold and can give a first order indication to designers on how much the mismatch is going to change in that region when different temperatures are involved.

5.4 Mismatch parameters

The mismatch performance of a device, or generally speaking of a process technology, is usually characterized through some device parameters, in this case: V_T, β and I_{ON}. Medians and sigmas of measured (extracted) parameters on the whole population are analyzed in this section and shown in table 5.2 while the behavior of the relative mismatch of I_{ON} will be studied on individual pair basis in the next one.

All the σ's of the aforementioned parameters have been calculated for all the populations at all the considered temperatures. The usual trend is a linear decline of the mismatch of these parameters, i.e., it decreases, when the temperature increases. For the sake of simplicity, in table 5.2 only the variation between the measured sigmas at the two extreme temperatures ($\sigma_{\Delta P}(125°C) - \sigma_{\Delta P}(0°C)$) is reported[1]. The "original" standard deviation, i.e., as measured at 25 °C, and 1-σ value of the short term repeatability, calculated as the standard

[1]Being a linear decline this difference is also the maximum swing measured.

Table 5.2: Summary of the change of the mismatch parameters over temperature and relative short term repeatability.

NMOS	C14			C90			C65			C45		
min length	$\delta\sigma_{\Delta P}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR
$\sigma_{\Delta V_{\mathrm{T}}}$ (mV)	-	13.1	± 1	-	12.0	± 0.6	-	19.1	± 1.3	-	18.7	± 2.1
$\sigma_{\Delta\beta/\beta}$ (%)	- 0.7	2.7	± 0.4	-	4.2	± 0.3	- 0.8	4.9	± 0.7	- 1.4	6.3	± 0.7
$\sigma_{\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}}$ (%)	-	1.7	± 0.02	- 0.2	2.7	± 0.05	- 0.2	3.0	± 0.06	- 0.5	5.0	± 0.4
NMOS	C14			C90			C65			C45		
1-μm long	$\delta\sigma_{\Delta P}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR
$\sigma_{\Delta V_{\mathrm{T}}}$ (mV)	-	5.0	± 0.3	- 0.4	4.6	± 0.15	-	4.5	± 0.3	- 1.2	8.4	± 0.4
$\sigma_{\Delta\beta/\beta}$ (%)	- 0.1	0.8	± 0.1	- 0.3	1.1	± 0.08	- 0.3	1.3	± 0.2	- 0.7	2.4	± 0.2
$\sigma_{\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}}$ (%)	- 0.1	1.0	± 0.01	- 0.1	1.0	± 0.02	- 0.1	1.1	± 0.06	- 0.2	1.6	± 0.03
PMOS	C14			C90			C65			C45		
min length	$\delta\sigma_{\Delta P}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR
$\sigma_{\Delta V_{\mathrm{T}}}$ (mV)	-	12.1	± 1.4	-	10.6	± 1.2	-	12.2	± 1.5	-	13.4	± 2.6
$\sigma_{\Delta\beta/\beta}$ (%)	-	2.6	± 0.6	-	3.0	± 0.5	-	3.4	± 1	-	5.2	± 0.8
$\sigma_{\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}}$ (%)	-	2.0	± 0.1	- 0.1	2.5	± 0.1	- 0.1	2.7	± 0.1	- 0.4	3.6	± 0.4
PMOS	C14			C90			C65			C45		
1-μm long	$\delta\sigma_{\Delta P}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR	$\delta\sigma_{\Delta \mathrm{P}}$	$\sigma_{\Delta P}$	STR
$\sigma_{\Delta V_{\mathrm{T}}}$ (mV)	-	3.2	± 0.6	- 0.7	4.4	± 0.3	- 1.0	4.1	± 0.5	- 0.5	3.3	± 0.5
$\sigma_{\Delta\beta/\beta}$ (%)	- 0.1	0.8	± 0.2	- 0.1	1.2	± 0.2	- 0.5	1.1	± 0.3	- 0.3	1.0	± 0.2
$\sigma_{\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}}$ (%)	- 0.1	0.8	± 0.04	- 0.1	0.8	± 0.04	- 0.1	0.9	± 0.1	- 0.1	0.8	± 0.1

When a clear trend is not visible over the whole temperatures range a dash ('-') is put instead of a number.

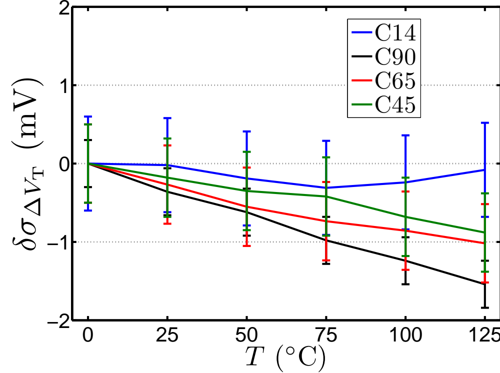


Figure 5.8: Variation of threshold voltage mismatch with respect to the ones measured at 0 °C of PMOS with 1 μm gate length for all four technologies. The error bars represent the measurement uncertainties (STR) as given in table 5.2.

deviation of the differences between consecutive observation at the same temperature and thus indicator of the measurement noise, are shown as well. No number, but a simple dash ('-'), has been put in the table when a **clear** trend was **not** visible across the six temperatures. An example is depicted in figure 5.8: the $\delta\sigma_{\Delta V_T}$ of long PMOS of C14. Two requirements had to be fulfilled to indicate a clear trend: the change of the value must be larger than the short term repeatability and the variation over temperature must be monotonous. The uncertainty associated with the limited population size (from temperature to temperature) is not taken into account because parameters extracted from the same population are compared and not general estimators. Figures 5.8 to 5.4.3 (excluding 5.9) are created using the data tabulated in Table 5.2. The variations of relative β and I_{ON} mismatch are depicted in figures for all dimensions and technologies. For the threshold voltage only one representative figure (the threshold voltage variation for the Long PMOS case) is shown and explained in the next section.

5.4.1 Threshold voltage mismatch

From the threshold voltage measurements it can be concluded that in most cases the threshold voltage mismatch does not vary with temperature. A significant change in $\sigma_{\Delta V_T}$ is appreciable only in transistors where the mismatch is higher than predicted by the simplest form of the Pelgrom model, i.e., when the long transistors show an area factor larger than the one calculated for the

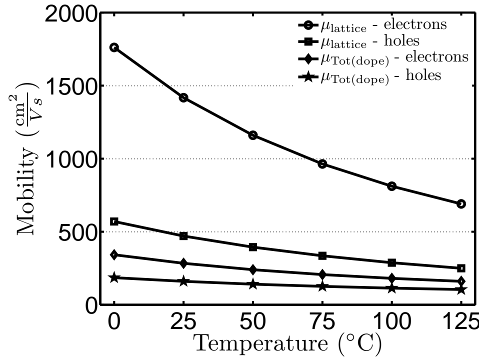


Figure 5.9: Comparison of mobility values at different temperatures for electrons and holes considering either only the lattice scattering or the doping dependence. The doping dependence was calculated following the expression in [102].

short ones. This is the case of the comparison shown in figure 5.8 where the differences of the threshold voltage mismatch at different temperatures, using the result obtained at 0°C as reference, are shown. For C14 no significant change in threshold voltage mismatch over temperature is visible. On the other hand, the other three technologies show an appreciable, i.e. larger than the STR (depicted in the graph with error bars), decrease of the threshold voltage mismatch. This is the case of technologies whose matching performance are slightly worsened by the presence of potential barriers at source and drain sides created by halo implantations [31, 89, 90]. In fact, an increase of the temperature will modify both the potential barrier heights and the energy of the carriers. The carriers will “see” smaller barriers thus reducing this extra contribution to the mismatch. Although this explains the observed reduction of $\sigma_{\Delta V_{\text{T}}}$ with higher temperatures, it should be noted that the variation, in any case, is very small and can be considered negligible for most uses.

5.4.2 Current factor mismatch

The current factor mismatch, however, shows a statistically significant decrease of the mismatch with temperature for all the devices and technologies except for PMOS devices with minimum gate length. The β factor is proportional to the W/L ratio, the gate capacitance, C_{ox}, and the mobility, μ. Of these only the latter is affected significantly by a change in temperature. According to the

standard MOSFET low-field mobility theory [99], at higher temperatures the scattering component associated with the silicon lattice becomes more important, reducing therefore the effect of the scattering component related to the dopants (major contributor to mobility mismatch). This is more pronounced for n-type than for p-type transistors.

This is depicted in figure 5.9 where the mobility for electrons and holes is calculated versus temperature in case of pure lattice scattering and taking into account the doping dependence. For the doping dependence the default model implemented in the simulator Sentaurus Device, the so-called Masetti model has been used [102]. A realistic doping concentration of $5 \cdot 10^{17}$ cm^{-3} was chosen for this calculation. It appears from the mobility values at different temperatures that the lowering of the mobility due to doping concentration with respect to the original lattice-scattering value, is substantially larger for electrons than it is for holes. This implies, thus, that the balance between the mobility components in NMOS (electrons) is more affected by a change in temperature. In other words, the component associated to the lattice scattering becomes more important for the overall mobility at high temperature for electrons than for holes. The underlying assumption is that the lattice-scattering component of the mobility does not contribute to the mismatch (or it contributes much less than the doping-caused component). The silicon lattice is exactly the same for all the devices and therefore the scattering associated with it should be uniform and equal to all, especially for devices in a matched pair. The component related to the doping reduction, on the other hand, will contribute more to the mobility mismatch.

5.4.3 I_{ON} mismatch

In a close relationship with β there is also I_{ON} mismatch. Also the relative mismatch fluctuation of this parameter, mostly used in digital design, tends to reduce with temperature. This trend is visible for all the dimensions, types and technologies with the exception of the short transistors fabricated in C14. The reduction of I_{ON} is the result of two simultaneous contributors, see equation (1.4): the reduction of the relative current factor mismatch and the increase of the gate overdrive.

The direct current measurement and the relatively high current involved resulted in a lower STR resulting in the capability of appreciating smaller trends for I_{ON} than for β. In case of C14 transistors the overdrive is much higher, see table 5.1, reducing the effect of the threshold voltage lowering. The impact of temperature on the I_{ON} mismatch in these devices is therefore negligible.

In figures from 5.10 to 5.13 the variations of $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}}$ with

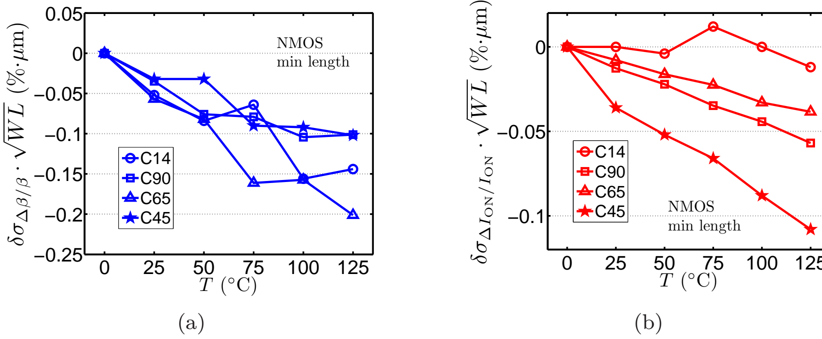


Figure 5.10: Variation of $\sigma_{\Delta\beta/\beta}$ (a) and $\sigma_{\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}}$ (b) with respect to the ones measured at 0 °C of NMOS with minimum gate length for all four technologies. The variations are multiplied to the square root of the active area.

respect to the one measured at 0 °C are plotted for all the dimensions, types and technologies. As the reader can notice, most of the plotted quantities show a negative change, i.e., an improvement of the mismatch standard deviations with temperature. The $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}}$ values related to minimum gate length transistors have been multiplied by the active area of the device for a fair comparison to the 1-μm device.

It is important to note the remarkable resemblance between the plots of β and I_{ON} for 1-μm long NMOSTs (see figure 5.11). This is an indication of the dominance of the low-field mobility component in those devices even when relatively high gate voltages are applied. The same does not happen for PMOSTs where the mobility mismatch, already at low fields, is less affected by the temperature. Summarizing, both $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}}$ show improved matching at higher temperatures. Although the changes are small they are consistent across all four technology nodes and device types.

5.5 Individual pair mismatch

Although it is reported in the previous section that I_{ON} mismatch standard deviations slightly decreases with an increase of temperatures, this does not mean that the mismatch of an individual pair reduces at higher temperature. In any case, since something seems to be happening with the mismatch of I_{ON} when considering the whole population, it is worthwhile to quantify the drift in temperature of an individual pair. This might be useful for high-precision circuits

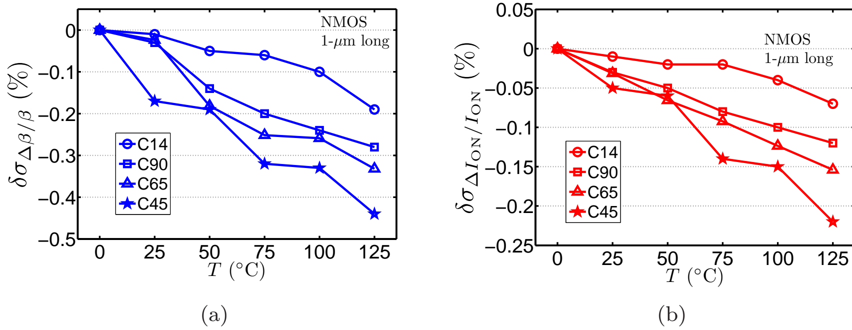


Figure 5.11: Variation of $\sigma_{\Delta\beta/\beta}$ (a) and $\sigma_{\Delta I_{ON}/I_{ON}}$ (b) with respect to the ones measured at 0 °C of 1-μm NMOS for all four technologies.

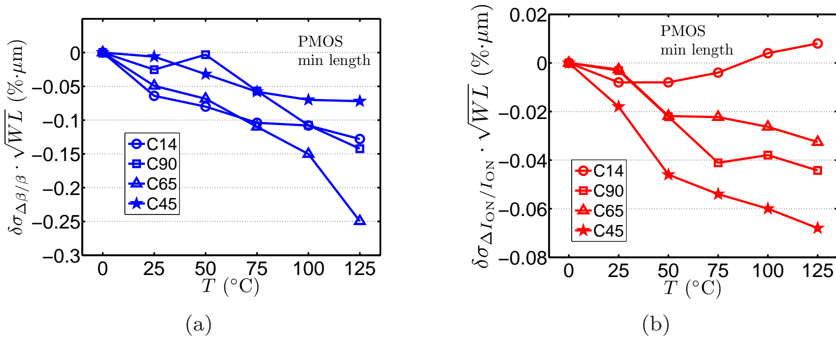


Figure 5.12: Variation of $\sigma_{\Delta\beta/\beta}$ (a) and $\sigma_{\Delta I_{ON}/I_{ON}}$ (b) with respect to the ones measured at 0 °C of PMOS with minimum gate length for all four technologies. The variations are multiplied to the square root of the active area.

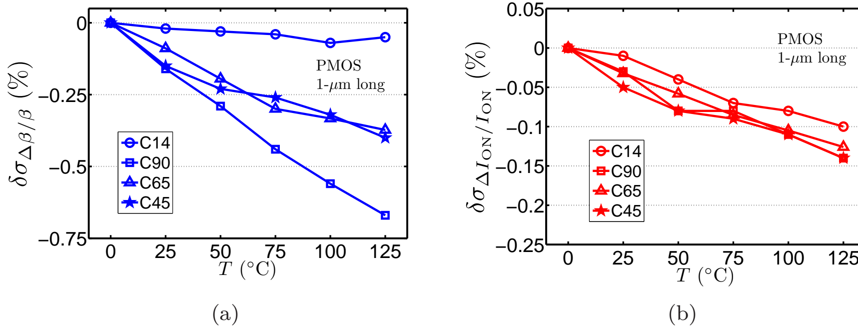


Figure 5.13: Variation of $\sigma_{\Delta\beta/\beta}$ (a) and $\sigma_{\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}}$ (b) with respect to the ones measured at 0 °C of 1-μm PMOS for all four technologies.

based on single-measurement (single-temperature) initial mismatch compensation.

As an example, the input offset voltage of a MOS differential pair is to first order described by the following equation:

$$V_{\mathrm{os}} = \Delta V_{\mathrm{T}} + I_{\mathrm{d}}/g_{\mathrm{m}} \times (\Delta g_{\mathrm{m}}/g_{\mathrm{m}}). \tag{5.2}$$

In [91] it is demonstrated that it is possible to compensate for the temperature variation of the ratio $I_{\mathrm{d}}/g_{\mathrm{m}}$ (the major contributor of the temperature drift of V_{os}) and remain only with the variation of threshold voltage mismatch and current factor relative mismatch. The same holds for mobility-based frequency references [92], where a compensation of the temperature variation of a frequency reference is done by using the temperature variation of the mobility and a temperature trimming. In these cases, the variation of the mismatch with temperature will represent a lower limit for the circuit performances.

In view of such considerations, it would be very useful to know the drift of the threshold voltage and the current factor mismatch with temperature. However, the actual drift of both is quite small, putting a severe challenge in terms of measurement capabilities. For the current factor mismatch a possible solution is to measure the drift of I_{ON} mismatch for each individual pair and consider it as an indication of the drift of the current factor mismatch. The threshold voltage mismatch, on the other hand, is somewhat more difficult to measure. In fact, no trend, larger than the short term repeatability, is visible for ΔV_{T} in individual pairs. That is why it was decided to focus, for individual pairs, only on the difference between the I_{ON} mismatch measured at different temperatures versus the one measured at 25 °C.

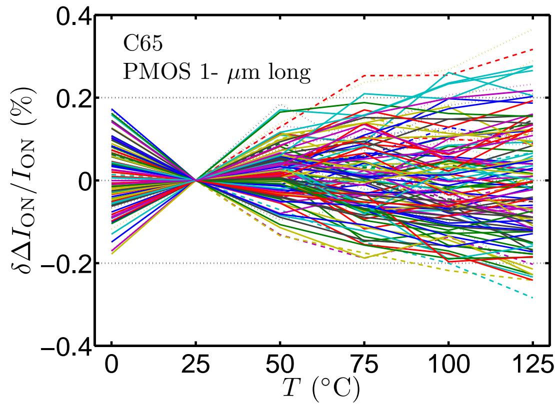


Figure 5.14: Every line represents the drift of $\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}$ of an individual matched pair with respect to the one measured at 25 °C (1-μm PMOS, C65). Differently from NMOS for the PMOS devices the individual pairs drift is clearly visible only over the full temperature range.

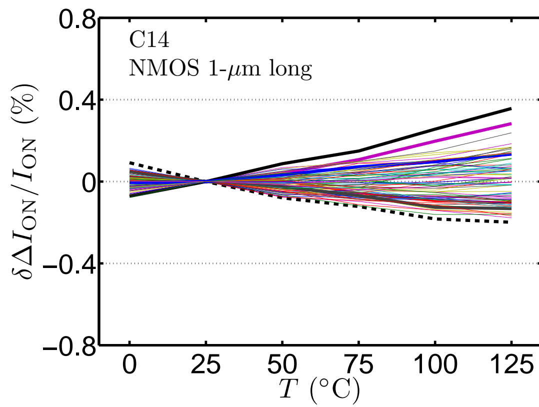


Figure 5.15: Every line represents the drift of $\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}$ of an individual matched pair with respect to the one measured at 25 °C (1-μm NMOS, C14).

It is observed that the correlation of mismatch observations within a population of pairs decreases with the increase of temperature difference. This implies that the two transistors of each pair do not react equally to a change

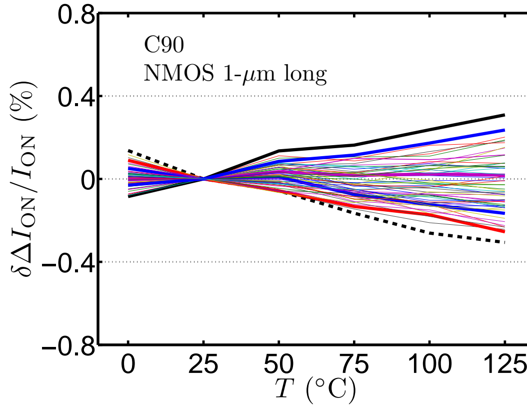


Figure 5.16: Every line represents the drift of $\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}$ of an individual matched pair with respect to the one measured at 25 °C (1-μm NMOS, C90).

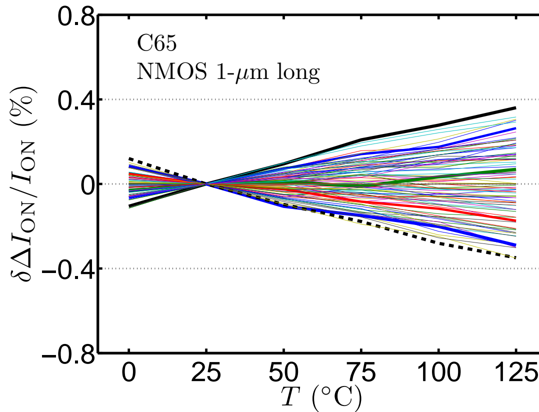


Figure 5.17: Every line represents the drift of $\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}$ of an individual matched pair with respect to the one measured at 25 °C (1-μm NMOS, C65).

of temperature. This is demonstrated in figures 5.15 to 5.18, where relative I_{ON} mismatch changes, using $\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}$ at 25 °C as reference, are shown for full populations of 1-μm long NMOST pairs for the four technologies. Every line in these figures represents an individual matched pair as measured on the

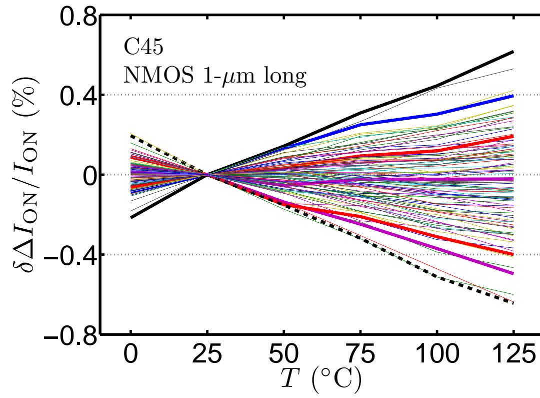


Figure 5.18: Every line represents the drift of $\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}$ of an individual matched pair with respect to the one measured at 25 °C (1-μm NMOS, C45).

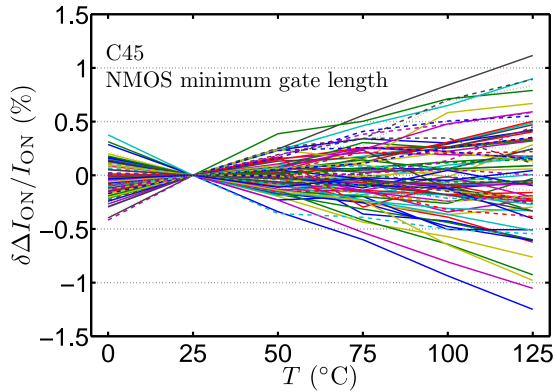


Figure 5.19: Every line represents the drift of $\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}$ of an individual matched pair with respect to the one measured at 25 °C (short NMOS, C45). The drift for the short transistors is roughly twice as much as the one observed for long transistors.

wafer. The temperature of 25 °C has been chosen as a reference to mimic a single-temperature trimming at room temperature. The long NMOSTs are the transistors with a clearer trend (being also the ones with the lowest STRs)

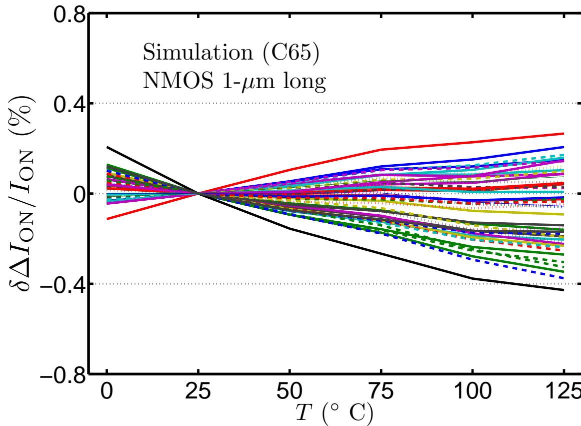


Figure 5.20: Every line represents the drift of $\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}$ of an individual matched pair with respect to the one measured at 25 °C (1-μm NMOS, simulated C65).

and moreover they are the ones that show a visible correlation between $\Delta\beta/\beta$ and $\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}$ (as it was already clear from figure 5.11). PMOSTs, on the other hand, show a non-consistent behavior among the four technologies and two dimensions. In most cases, in fact, a clear drift is distinguishable only over the full range of temperature, the small drift at lower temperature, if present, is hidden by the short term repeatability (see as example figure 5.14).

For all technologies mismatch drift is present and follows a clear, linear trend. This drift is predominantly attributed to mobility differences associated with random dopant differences, i.e., the temperature coefficient of the mobility may vary slightly from transistor to transistor leading to a different change of the current versus temperature. This was confirmed using SiSPET. In fact using the same devices as described in chapter 3 (the virtual copy of C65), the I_{ON} was simulated at six temperatures. RDF was the only source of fluctuation introduced for these simulations. The results are shown in figure 5.20. The trend and the magnitude are remarkably similar to the measured one. The dependency on the doping of the temperature coefficient of the mobility model can explain this kind of behavior for these particular simulations. It is an excellent demonstration of the theory behind this drift and ultimately of the validity and usefulness of the simulation approach.

It is worth to notice that although the dimensions of the transistors shown in figures 5.15 to 5.18 are the same (W/L=1 μm/1 μm) an increase of the drift

with the advance of the technology (with a major increase in C45) is visible. Indeed, the difference of ΔI_{ON} over 100 °C can, for C45, be twice as much as it is for C14, ±0.007 %/°C and ±0.0035 %/°C. This might be due to the presence of strain in this particular technology and the presence of enhanced potential barriers that slightly modify the threshold voltage mismatch. Further experiments would be necessary to confirm these assumptions.

For minimum gate length NMOSTs the trend is also quite visible (although still hampered by a worse STR) and shows a maximum drift that is approximately twice as much as the one observed for the longer transistors (see the case of C45 in figure 5.19).

Design consequences

Another way to look at this effect is to translate the current mismatch in an input referred offset voltage, i.e., the additional gate-source voltage needed to compensate the relative current mismatch, using the following equation:

$$\Delta V_{\mathrm{in}} = 0.5(\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}) \cdot (V_{\mathrm{gs}} - V_{\mathrm{T}}) \tag{5.3}$$

Thus, according to 5.3 and taking the $\delta\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}$ from table 5.2 the drift seen in 1-μm long NMOS pairs can be, in the worst case, as large as about $\pm 15\ \mu V/°\mathrm{C}$ (C45 case). Once again, although the observed effects may seem small, it should be realized that this effect puts severe limitations on the application of high-precision trimmed circuits when the system's operating temperature is not equal to the trimming temperature.

5.6 Conclusion

In this chapter we have presented extensive mismatch measurements over a substantial temperature range on four different technology nodes covering both n- and p-type transistors and for two different gate lengths.

The mismatch of the main transistor parameters does not change significantly over temperature even though the current factor and I_{ON} matching show a slight improvement at higher temperatures.

An elaborate analysis on subthreshold mismatch does show a significant reduction of current mismatch with increasing temperature, but this is understandable using elementary device models.

However, it is shown and demonstrated with simulations that the mismatch of individual pairs can drift, hence resulting in changes of the mismatch that can defy the fundamental current mismatch fluctuation improvement trend in

case of trimmed circuits. As future work, it would be useful to extract a scaling rule also for the drift of ΔI_{ON} and use a more reliable method to quantify the drift of the threshold voltage mismatch in order to extract (if present) the change of ΔV_{T} over temperature. Furthermore, it is of importance to establish the relation between $\Delta I_{\mathrm{ON}}/I_{\mathrm{ON}}$ mismatch and $\Delta\beta/\beta$ at low-field conditions in order to obtain useful and trustworthy numbers for analog designers.

Chapter 6

Conclusions

In this thesis, an interpretation of mismatch signature of contemporary MOS transistors has been given through statistical simulations and dedicated measurements. This research has been conducted in the NXP Semiconductors research department. Since this is an industrial research environment, rather than an academic one, the choice of subjects was inevitably affected by the business direction of the company. The investigation was thus directed towards improvement of the understanding of the mismatch dynamics in actual production devices (CMOS and LDMOS) and focused on intrinsic sources of fluctuations (random doping fluctuations, interface state fluctuations) as well as possible environmental variables (temperature, series resistances).

This project demonstrates beyond any doubt the value of statistical device simulations for interpreting subtle device effects during process development and high precision modeling of contemporary MOS devices.

Initially, a statistical 2-D device simulation suite has been expanded and tested extensively. It has been shown that, once the limitations of the simulation tools have been established, a two-dimensional simulation can give reliable results and help the understanding process of mismatch physics dynamics. As a part of the whole procedure of setting up a trustworthy simulator, the TCAD calibration of a modern NMOS device has been discussed (chapter 2).

This well-tuned simulator represented the base for the study of the effect of random dopant fluctuations and interface state fluctuations on MOS transistor mismatch. In fact, through a new analysis method, based on mismatch signatures, PCA and statistical device simulations, it has been demonstrated that interface state fluctuations can be responsible for a large part of the measured

drain current mismatch. The simulation using only RDF and the measurements obtained on matched pairs show a clear difference in subthreshold and moderate inversion, the region where the interface states can affect the mismatch the most (chapter 3).

Furthermore, focusing on the behavior of the device in subthreshold, a shortcoming of the current implementation of the mismatch in compact model was identified. A better description is obtained by letting fluctuate a further parameter, related to interface states. One of the main points visible in measurements and RDF&RIF simulations is that the relative drain current mismatch in subthreshold is not fully correlated with the mismatch at threshold voltage. With a simple two-parameter approach this signature is impossible to replicate as one parameter will control the mismatch at threshold and below while the second will influence only the mismatch in strong inversion (chapter 3).

Subsequently, a successful microsecond pulsed DC MOSFET matching measurements down to nano-amperes current levels has been reported. This was used to study MOSFET mismatch in weak inversion under pulsed DC conditions so to have more insights on the properties of these interface states. The experiment suggests that the interface states must be faster than 1 μs, if they really contribute substantially to the mismatch in contemporary advanced CMOS technologies. In any case, this was the first reported attempt of a very-fast pulsed mismatch characterization down to sub-micro ampere level (chapter 3).

Beside MOSFETs, the simulator and the statistical data analysis technique have been applied to LDMOS devices. Measurements on transistor pairs show relatively large drain current mismatch fluctuations in all regions of operation. It has been found that, if only random dopant fluctuations are taken into account, the shape and level of the channel doping cannot explain the observed mismatch behavior. On the other hand, random interface states significantly affect the behavior of the device in subthreshold as well as in moderate inversion due to the lateral non-uniformity of the channel doping. It has also been shown that, due to the relatively high current involved during the operation of this kind of device, particular care must be taken to avoid series resistances to hamper both measurement and matching properties during operation (chapter 4).

Finally, an extensive characterization of mismatch over temperature has been presented. The mismatch of the main transistor parameters does not change significantly over temperature even though the current factor and I_{ON} matching show a slight improvement. This is shown for four different technology nodes highlighting also the trend and the differences visible across them.

An elaborate analysis on subthreshold mismatch does show a significant reduction of current mismatch with increasing temperature in line with a simple model that explains the physical background of this effect. However, we have demonstrated with extensive measurements and confirmed with device simulations that the mismatch of individual pairs can drift, hence resulting in changes of the mismatch that can defy the fundamental current mismatch fluctuation improvement trend in case of trimmed circuits (chapter 5).

All in all, it can be concluded that this work has successfully explored the limits of the capabilities of the 2-D DD statistical simulations as a tool for investigating and interpreting random device fluctuations in MOS transistors. During this research project, many insights have been obtained that help to understand the impact of microscopic device architecture fluctuations. Some basically known effects have been properly quantified, and some new effects have been encountered and duly presented to the scientific world.

6.1 Future work

The development of a tool as described in this thesis (and its predecessor by Ewert [18]) is not (never) finished; neither is the interpretation of mismatch signatures in contemporary MOS technologies by any means completed. Further work on SiSPET is required to come to better implementation of the energy/density distribution in the context of random interface states fluctuations. Simulation of PMOS transistors has not even been attempted yet in this framework.

Another open end lies in the interpretation of the impact of high dose halo's (resulting in strong channel-dopant non-uniformities) in relation to length scaling of mismatch and associated temperature effect. Further investigations for identifying optimal halo doping profiles for different transistor types and their impact on the mismatch signatures will be required to come to better interpretation and modeling of long-channel devices in contemporary and future process nodes [90, 89]. Moreover, the literature and the everyday practice of characterization of variability in advanced IC technologies provide a whole range of microscopic device architecture fluctuation effects that could (should?) be studied in more depth and properly quantified for optimized design of advanced electronic circuits and systems.

Subjects like source and drain doping fluctuations, gate granularity, work function fluctuations, line edge roughness, and high k dielectric composition fluctuations provide fruitful challenges for advanced statistical device simulations. Techniques for including more device fluctuation effects and their corre-

lations into compact models like PSP have merely been touched upon in this work. Both for the implementation into the compact model equations and geometric preprocessing blocks, and optimal parameter extraction strategies, major improvements can be made and substantial benefits can be expected for advanced mixed-signal circuit design optimization techniques.

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Samenvatting

Het is onmogelijk om twee exact gelijke transistoren te fabriceren. Microscopische verschillen in de opbouw van iedere transistor leiden onvermijdelijk tot kleine verschillen in hun elektrische prestaties. Het elektrische prestatieverschil tussen twee a-priori identiek veronderstelde transistoren, een zogenaamd *matched pair*, wordt aangeduid met de term *mismatch*. Ten gevolge van natuurlijke fluctuaties in de dichtheden van transistor constructie elementen zoals doteringsatomen en, al dan niet met opzet, aangebrachte ladingen in de transistoren blijkt deze mismatch stochastisch te fluctueren. De hoofdfunctionaliteit van diverse elektronische bouwblokken wordt gebaseerd op het toepassen van identieke componenten (*devices*). Met het afnemen van de afmetingen van componenten worden deze verschillen meer geprononceerd. Dientengevolge is het karakteriseren en modelleren van mismatch een van de belangrijkste elementen van zowel het fabricage- als het ontwerpproces van moderne geïntegreerde schakelingen (*chips*). In dit proefschrift wordt MOS transistor mismatch bestudeerd door middel van statistische device simulaties. In het bijzonder worden gesimuleerde en gemeten representaties van het mismatchgedrag vergeleken door middel van zogenaamde *mismatch signatures*.

Deze worden gevormd door de combinatie van de grafiek van de standaard afwijking van de relatieve drainstroom mismatch fluctuatie als functie van de volledige beschikbare spanningsslag, en een grafiek van correlatie tussen de drainstroom mismatches bij een willekeurige gatespanning met degenen zoals berekend bij een gatespanning gelijk aan de drempelspanning van de MOS transistor.

Het belang van mismatch analyse in de fabricage van moderne halfgeleiders, en een overzicht van de literatuur op dit gebied worden geïntroduceerd in hoofdstuk 1.

Het belangrijkste gereedschap dat door dit hele proefschrift heen veelvuldig gebruikt wordt, een 2-D drift-diffusie simulator met de mogelijkheid om willekeurige statistische fluctuatie in de berekende componenten aan te brengen, wordt geïntroduceerd en bediscussieerd in hoofdstuk 2. In dit hoofdstuk wordt ook de gebruikte analysemethode beschreven. Het complete simulatiesysteem, SiSPET geheten, is gebruikt om de mismatch gedragingen van gemeten matched pair teststructuren te vergelijken met gesimuleerde (berekende) resultaten van goed nagebootste replica's van de transistoren. De analysemethode is gekozen om een brede evaluatie van de mismatch prestaties te verkrijgen. Hiervoor is gekozen voor de techniek van het gebruiken van mismatch signatures. Deze resulteren niet alleen in een gelijktijdige analyse van kwantitatieve zowel als kwalitatieve aspecten van mismatch, maar blijken ook geschikt voor het identificeren van subtiliteiten die over het hoofd gezien zouden worden bij toepassing van de klassieke puur kwantitatieve methode (bijv. via ΔV_{T} en $\Delta\beta/\beta$ vergelijking).

In hoofdstuk 3 worden de effecten van *interface states* (toestanden) op MOS transistor mismatch bestudeerd. Door middel van de analyse van mismatch signatures van moderne MOSFETs laat dit werk zien dat er, naast de traditionele veronderstelde hoofdoorzaak gerelateerd aan random doteringsfluctuaties (RDF), een onafhankelijke oorzaak van mismatch bestaat die het fluctuatieniveau in het zwakke inversiegebied (*subthreshold*) domineert. Door middel van statistische simulaties wordt aangetoond dat interface states tussen het gate dielectricum en het silicium sterk, en kwalitatief correct, bijdragen aan de mismatch in het genoemde stroomgebied, indien zowel de dosis en de positie, als het energieniveau van de interface states gerandomiseerd worden. Daarbovenop wordt getoond dat de mismatch signatures niet gereproduceerd kunnen worden met de conventionele twee-parameter aanpak zoals gebruikelijk in de huidige statistische circuit simulatie modellen. Een derde, statistisch onafhankelijke, parameter blijkt nodig om de statistische representatie van het mismatch gedrag te verbeteren.

Diverse vervolgexperimenten werden uitgevoerd om de effecten van interface states op mismatch verder te onderzoeken. Een alternatief algoritme voor de randomisering van de energieniveaus van de interface states werd geïmplementeerd in SiSPET, maar dit bleek te resulteren in een verminderd effect van de fluctuaties van interface states op transistor mismatch. Dit resultaat toont een beperking van het gebruik van 2-D simulatoren voor het simuleren van inherent driedimensionale effecten. Tegelijkertijd werden de effecten van interface states' fluctuaties getest door metingen met gepulste I-V metingen. Het doel hiervan was om de bijdrage van snelle *traps* te isoleren van de mismatch die toegewezen kan worden aan random doping fluctuaties. Aangezien geen signif-

icante verschillen aangetoond konden worden tussen gepulste metingen en de standaard DC metingen, kan geconcludeerd worden dat de interface states die bijdragen aan de mismatch sneller zijn dan 1 micro seconde, of dat zij minder belangrijk zijn dan gesuggereerd door de eerdere simulaties.

In hoofdstuk 4 staat beschreven hoe de simulatie- en analysemethodes gebaseerd op mismatch signatures toegepast kunnen worden om het mismatch gedrag te bestuderen van een ander type transistoren: de enkelzijdig lateraal gediffundeerde MOS transistor (LDMOST). Dit type van transistoren vertoont een hogere mismatch dan voorspeld op basis van de theorieën gebaseerd op conventionele symmetrische transistorarchitecturen. Door vergelijking van simulaties en metingen wordt gedemonstreerd dat ook dit type transistoren sterk beïnvloed wordt door interface states fluctuaties, versterkt door de laterale niet-uniformiteit van de kanaaldotering. Tevens laat deze studie zien dat de mismatch metingen serieus verstoord kunnen worden door fluctuaties van de serie-weerstand, voornamelijk door de relatief hoge stromen dat dit soort transistoren kan leveren.

In hoofdstuk 5 wordt de invloed bestudeerd van de omgevings- of chiptemperatuur op mismatch, door middel van uitgebreide statistische metingen voor twee kanaaltypes (NMOSTs en PMOSTs), ieder met twee transistorafmetingen, over vier technologiegeneraties. Hoewel de belangrijkste indicatoren van MOS transistor mismatch, te weten $\sigma_{\Delta V_\mathrm{T}}$ en $\sigma_{\Delta\beta/\beta}$ niet sterk afhankelijk blijken te zijn van de temperatuur, blijkt de mismatch in zwakke inversie substantieel te veranderen. Tevens wordt getoond dat de $I_{(ON}$ mismatch van individuele matched pairs weg kan driften in a-priori niet voorspelbare richting. Deze niet eerder gerapporteerde waarneming betekent dat circuitontwerpen die gebruik maken van ingebouwde kalibratietechnieken de opgeslagen compensatie moeten aanpassen tijdens of na temperatuurveranderingen.

Tot besluit worden in het laatste hoofdstuk de belangrijkste conclusies van dit proefschrift samengevat en worden enige aanwijzingen gegeven voor de te volgen richtingen ten behoeve van mogelijke vervolgstudies.

Summary

It is impossible to fabricate two exactly identical transistors. Microscopic device architecture differences will lead to slightly different electrical performance. The electrical performance difference between two a-priori assumed identical transistors, a matched pair, is indicated with the term mismatch. Due to the natural fluctuation of the microscopic construction elements of transistors, such as dopant atoms and built-in charges, mismatch shows stochastic fluctuations. Many fundamental electronic circuit blocks base their functionality on the utilization of identical devices. With the shrinking of device dimensions these differences become even more pronounced. As a consequence, the characterization and modeling of the mismatch is one of the most important part of contemporary chip fabrication/design process.

In this thesis, MOS transistor mismatch was studied through statistical device simulations. In particular, simulated and measured so-called *mismatch signatures* have been compared. Mismatch signatures are the combination of the standard deviation of the relative drain current mismatch fluctuation over the full bias range and the correlation of the drain current mismatch at any gate bias with the one observed at threshold voltage.

The importance of mismatch analysis in contemporary semiconductor fabrication and a literature review of mismatch are presented in chapter 1. The main tool used throughout the thesis, a 2-D drift-diffusion simulator with randomization capabilities, is introduced and discussed in chapter 2. In this chapter the analysis method is also described. The simulator tool, called SiSPET, was used to compare the mismatch behaviors as measured on dedicated matched pair test structures with those simulated on well-calibrated replicas of the same devices. The analysis method has been carefully chosen in order to obtain a comprehensive evaluation of the mismatch performance. Mismatch signatures

were created with this purpose. These signatures not only allow a quantitative and qualitative analysis at the same time but are also suitable for highlighting subtleties that would be overlooked with a purely quantitative approach (e.g., ΔV_{T} and $\Delta\beta/\beta$ comparison).

In chapter 3 the impact of interface states on MOS transistor mismatch is studied. Through mismatch signatures analysis on contemporary MOSFETs it has been proven that there is a cause of mismatch, independent from the random dopant fluctuations, that dominates the mismatch in subthreshold. Using statistical simulations it was demonstrated that interface states between the gate oxide and silicon, if randomized in terms of concentration, energy and position can heavily contribute to the mismatch in the aforementioned region. Moreover, it was shown that the mismatch signature could not be replicated with the standard two-parameter approach of present compact modeling. A third parameter, independent from the other two, was necessary to improve the statistical representation of the mismatch behavior.

Further experiments were performed to investigate the role of interface states in mismatch. A different randomization of the interface states energy was implemented in the simulations, resulting in a reduced effect of the interface states fluctuations on mismatch. This result showed the limit of 2-D simulators when trying to simulate inherent 3-D effects. At the same time, the impact of interface states fluctuations was tested through very-fast pulsed I-V measurements. The aim was to isolate the contribution of fast traps from the random dopant fluctuation related mismatch. Since no clear difference was found between fast pulsed measurements and the standard DC measurements, it can be concluded that either the interface states that contribute to mismatch are faster than 1 μs or they are less important than the first simulation would imply.

In chapter 4 the simulation and analysis method, based on mismatch signatures, were applied to study the mismatch behavior of a different type of device: a Lateral Diffused MOS. These devices show a larger mismatch than bulk MOS theory predicts. By comparing simulations and measurements it was demonstrated that these devices are heavily affected by interface state fluctuations due to their laterally non-uniform doped channel and that measurements can be seriously hampered by series resistance fluctuations due to the relatively high currents that they deliver.

In chapter 5 the impact of temperature on mismatch has been studied with extensive measurements across four technology nodes and two channel types and dimensions. Although the main indicators of the MOS transistor mismatch performance, such as $\sigma_{\Delta V_{\mathrm{T}}}$ and $\sigma_{\Delta\beta/\beta}$, do not vary significantly with temperature, the mismatch in subthreshold changes substantially and the relative I_{ON}

mismatch of individual matched pair can drift. These previously unreported observations imply that circuit designs employing mismatch compensation techniques should adjust the compensation upon a temperature change.

Finally, in the last chapter the main conclusions of the thesis are summarized and possible future directions for this work are indicated.

About the author

Biography

Pietro Andricciola was born in Venafro, Italy, on April 24th 1982. He received the B.Sc. and M.Sc. (cum laude) degrees in Electrical Engineering from the University of Napoli "Federico II", Italy, in 2004 and 2006, respectively. His master's thesis was carried out within the Delft Institute of Microsystems and Nanoelectronics (DIMES), Delft, The Netherlands, as part of an Erasmus exchange project. After graduation, he spent six months of internship working on the characterization of phase change memory in NXP Research, Leuven, Belgium.

Between 2007 and 2011, he was employed as Marie Curie Fellow in the Device Modeling and Characterization group of NXP Semiconductors' Central R&D. There he carried out his Ph.D. research in partnership with the group of Semiconductor Components of University of Twente. His research interests were focused on the interpretation of variability and mismatch in modern CMOS technologies through measurements and statistical TCAD simulations.

Since June 2011, he is an application and business support engineer at ASML B.V. in Veldhoven, The Netherlands.

List of publications

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- **P. Andricciola**, and H. P. Tuinhout, "The temperature dependence of mismatch in deep-submicrometer bulk MOSFETs", *IEEE Electron Device*

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- **P. Andricciola**, and H. P. Tuinhout, “Influence of halo doping profiles on MOS transistor mismatch”, *Semiconductor Advances and Future Electronics workshop*, Veldhoven (NL), November 2009.

- **P. Andricciola**, and H. P. Tuinhout, “Trends and differences of the temperature effect on mismatch in different CMOS technology nodes”, *Semiconductor Advances and Future Electronics workshop*, Veldhoven (NL), November 2010. **Invited for a plenary talk**

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By the way, if you, reader, reached the end, you did not find your name and you feel you should have been here, please accept my apologies and my late acknowledgment.

Eindhoven, December 2011,
Pietro Andricciola